

BAD50_HC

DIS/UMA/Muxless Schematics Document

IVY/SNB Bridge

Panther Point

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC885 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Core Design>

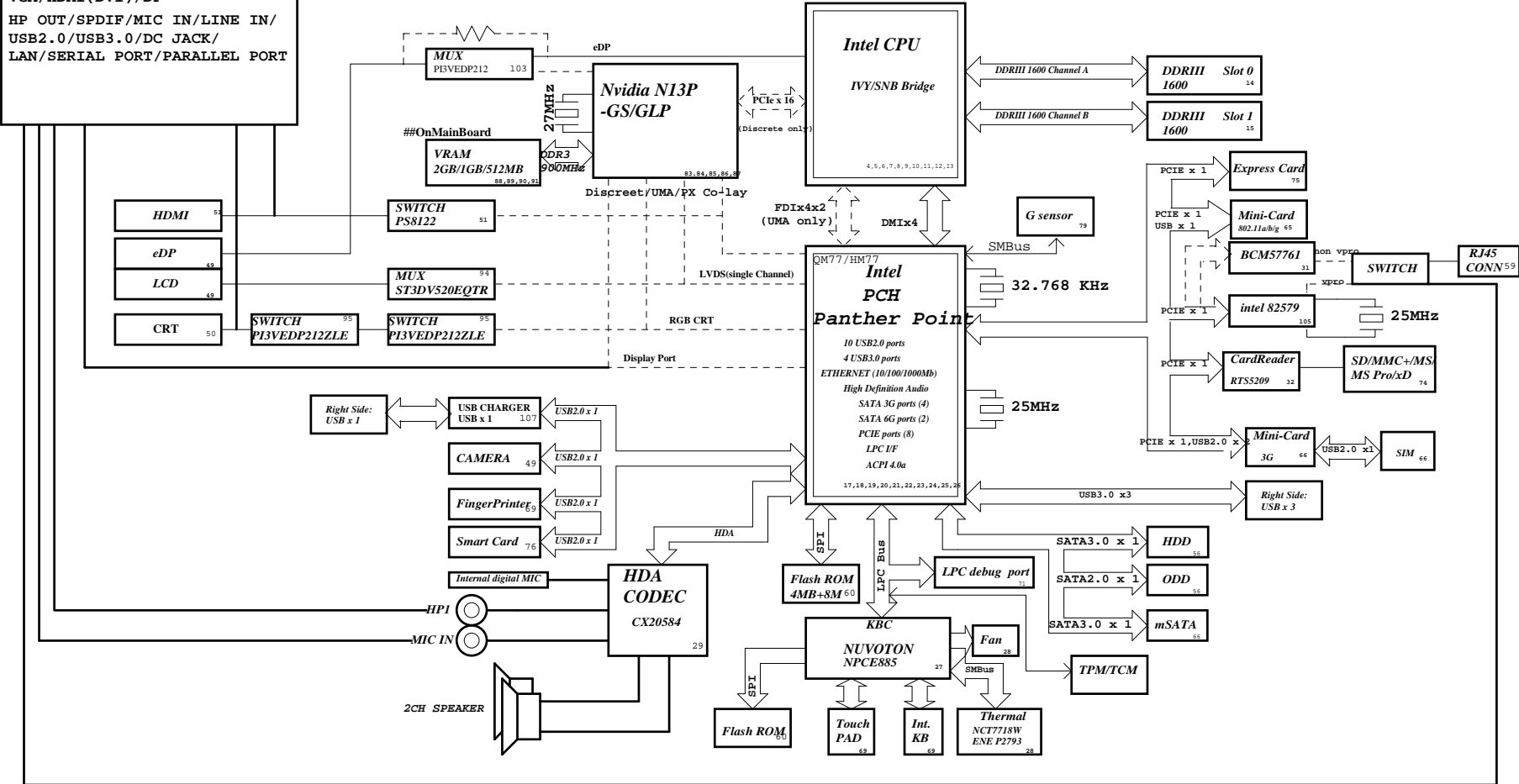
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Title					
Cover Page					
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BAD50-HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4UP01.001
Project Name: BAD50_HC
PCB No:11288
PCB Version: -1

Buttom Docking

VGA/HDMI (DVI) /DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



TI CHARGER BQ24707		40
INPUTS	DCBATOUT	
OUTPUTS	BT+	
SYSTEM DC/DC RT8239CGQW		41
INPUTS	DCBATOUT	
OUTPUTS	SV_AUX_S5 3D3V_AUX_S5 SV_CHARGER 3D3V_S5	
CPU DC/DC ISL95831HRTZ		42-43
INPUTS	DCBATOUT	
OUTPUTS	VCC_CORE	
GFX DC/DC ISL95831HRTZ		44
INPUTS	DCBATOUT	
OUTPUTS	+VCC GFXCORE	
SYSTEM DC/DC TPS51218DS		45
INPUTS	DCBATOUT	
OUTPUTS	1D05V_LAN	
SYSTEM DC/DC RT8207LGQW		46
INPUTS	DCBATOUT	
OUTPUTS	1D05V_S3 0D75V_S0	
SYSTEM DC/DC APW7153B		47
INPUTS	3D3V_S5	
OUTPUTS	1D05V_S0	
SYSTEM DC/DC TPS51461		48
INPUTS	SV_S5	
OUTPUTS	0D85V_S0	
VGA VT1312MPQX		92
INPUTS	SV_PWR	
OUTPUTS	VGA_CORE	
Switches		
INPUTS	OUTPUTS	
SV_CHARGER	SV_S5	
Switches		
INPUTS	OUTPUTS	
1D05V_S3	1D05V_VGA_S0	
3D3V_S0	3D3V_VGA_S0	
PCB LAYER		
L1:Top	L5:Power	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

<Core Design>

PCH Strapping Chief River Schematic Checklist Rev1.5

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: If the signal is sampled high.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high. External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor.
DF_TVS	A strap for selecting DMI and FDI termination voltage. DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms $\pm 5\%$ resistor.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts.
SATA2GP/ GPIO36	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_SDO	Weak internal pull-down. This signal has a 20k internal pull down resistor.
HDA_SYNC	On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down
SDVO_CTRLDATA DDPC_CTRLDATA DDPD_CTRLDATA	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down
DSWVRMEN	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	If not used, 8.2-k Ω to 10-k Ω pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting when use as the chipset test interface.
GPIO29/ SLP_LAN#	If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN. If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO.

USB Table

PCIE Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN
LANE7	New Card
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	M-SATA
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	USB port 1
1	USB port 2
2	USB port3 (usb charger)
3	Dock
4	X
5	Fingerprint
6	smart card
7	X
8	Mini Card2 (WWAN)
9	USB port4(ESATA),on M/
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connect to the EMBEDDED display Port	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	configuration lands. A test point may be placed on the board for these lands.		

POWER PLANE		VOLTAGE	Voltage Rails		DESCRIPTION
			ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1.5V 1.05V		S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V		S3		
BT+ DCBATOUT 5V_S5 5V_CHARGER 5V_AUX_S5 3D3V_S5	7V-19.5V 7V-19.5V 5V 5V 5V 3.3V		All S states		AC Brick Mode only
3D3V_AUX_S5 3D3V_LAN_S5	3.3V 3.3V		WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V		DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V		G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		CHIEF RIVER ORS	
Device	Address	Bus	
EC SMBus 1			
Battery 0	0x16	BAT_SCL/BAT_SDA	
CHARGER	0x12	BAT_SCL/BAT_SDA	
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA	
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA	
EC SMBus 2			
Battery 1	0x16	SM1L_CLK/SM1L_DATA	
PCB	0x96 & 0x94	SM1L_CLK/SM1L_DATA	
Discrete VGA Thermal	0x9C or 0x9E	SM1L_CLK/SM1L_DATA	
PS8321 HDMI level shifter	0x96 & 0x97	SM1L_CLK/SM1L_DATA	
NCT771BW	0x98 or 0x99	SM1L_CLK/SM1L_DATA	
EC SMBus 3			
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA	
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA	
PCH SMBus			
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK	
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK	
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK	
G-Sensor		PCH_SMBDATA/PCH_SMBCLK	
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK	
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK	

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SSID = CPU

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

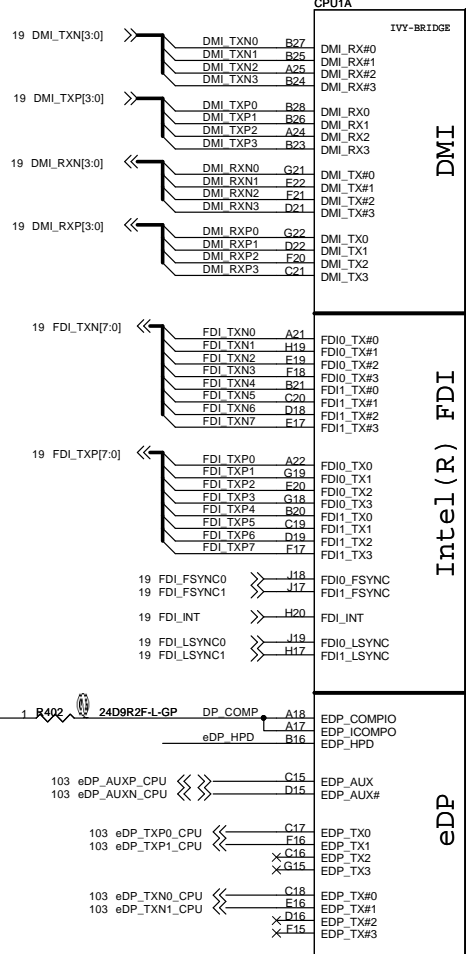
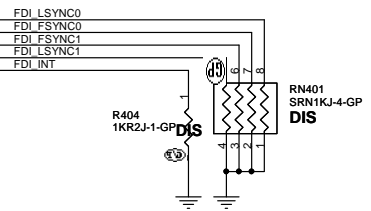
Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

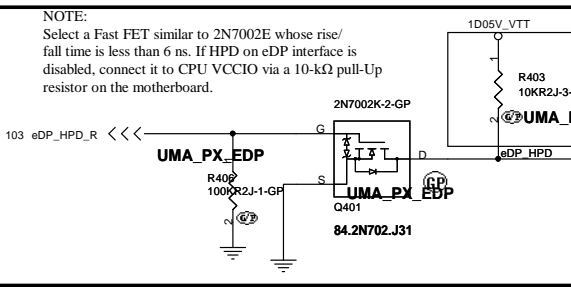
NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.



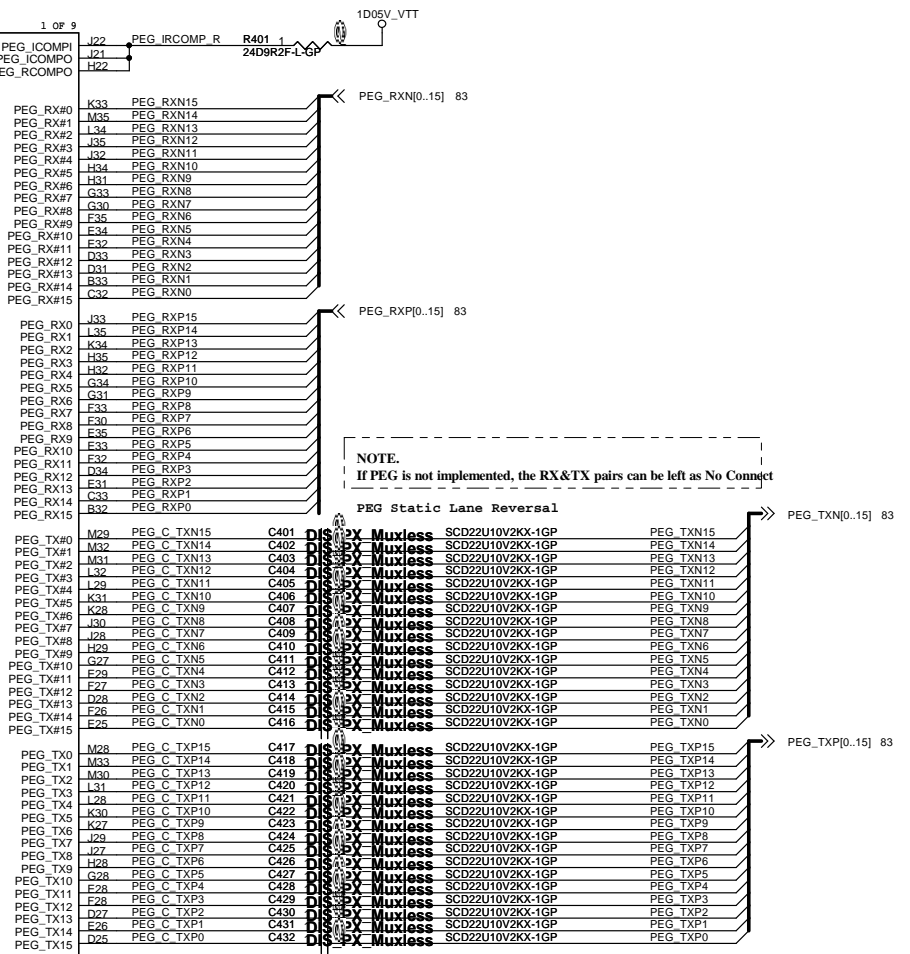
NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

62.10055.321



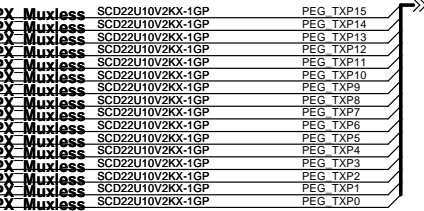
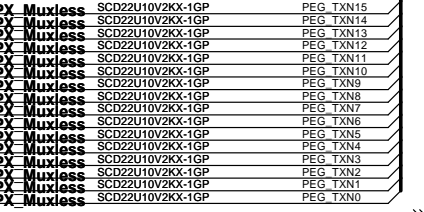
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

PCI EXPRESS* - GRAPHICS



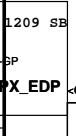
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

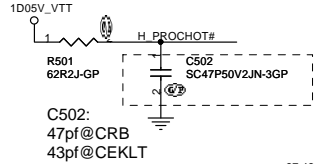


全改MUX

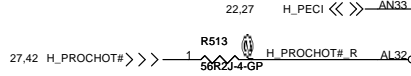
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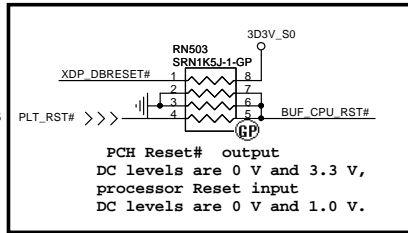
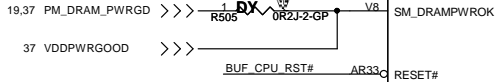
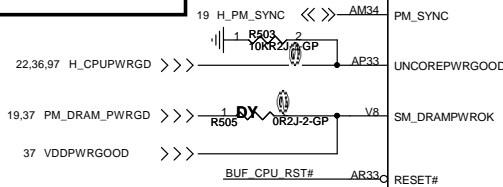


CATERR#
this signal should have
an exposed test point for
easy debug access.

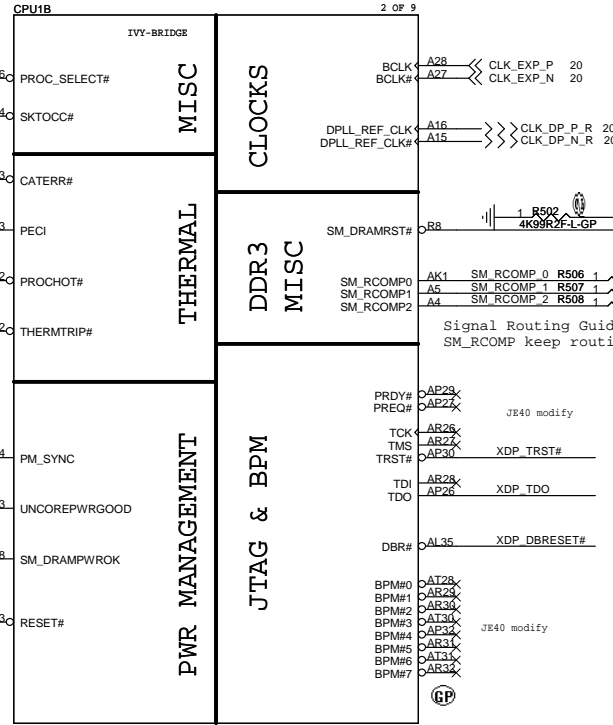


Connect EC to PROCHOT# through inverting OD buffer.

PROCHOT# with Two VR topology:
Requires a series-resistor of 100 $\pm 5\%$
close to the processor followed by a
75 $\pm 5\%$ pull-up to VTT power-rail towards the VR.
A pull up to VCCP(1.05 V)
through 300 $\pm 5\%$ resistor close to the IMVP 7

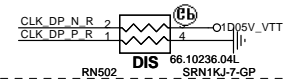


PCH Reset# output
DC levels are 0 V and 3.3 V,
processor Reset input
DC levels are 0 V and 1.0 V.

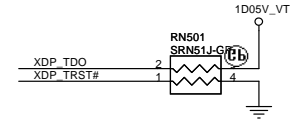


62.10055.321

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K $\pm 5\%$ resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K $\pm 5\%$ resistor power (~15 mW) may be
wasted.



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



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CPU (THERMAL/CLOCK/PM)		
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SSID = CPU

CPU1C

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IVY-BRIDGE

DDR SYSTEM MEMORY A

62.10055.321

CPU1D

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IVY-BRIDGE

DDR SYSTEM MEMORY B

62.10055.321

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Title

CPU (DDR)

Size

A3

Document Number

BAD50-HC

Rev

-1

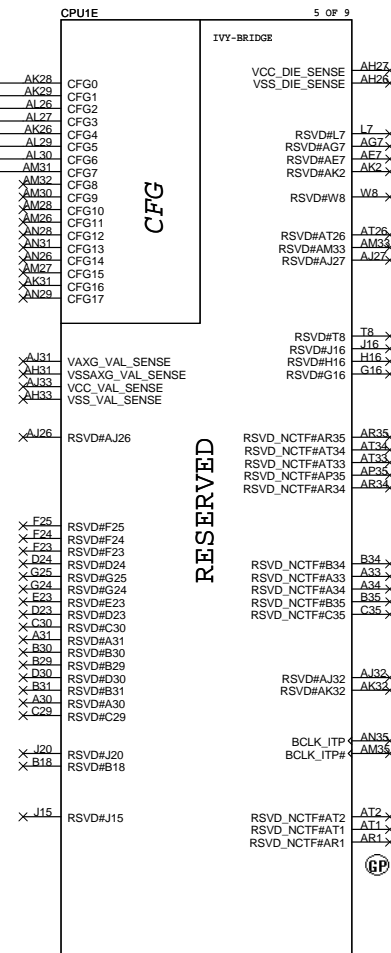
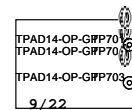
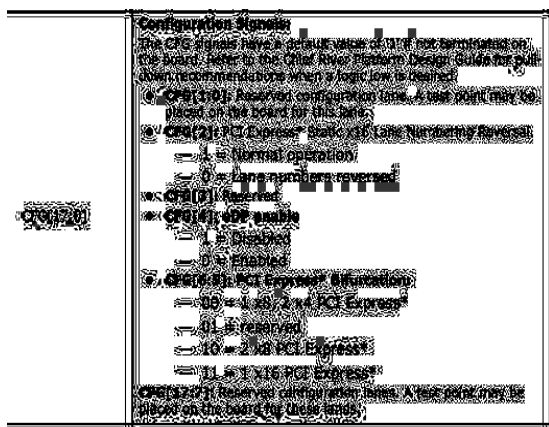
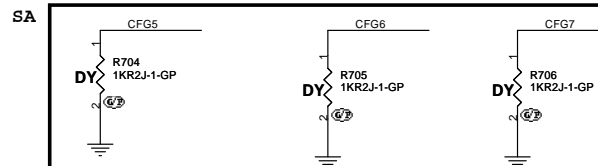
Date: Friday, March 02, 2012

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PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



<Core Design>

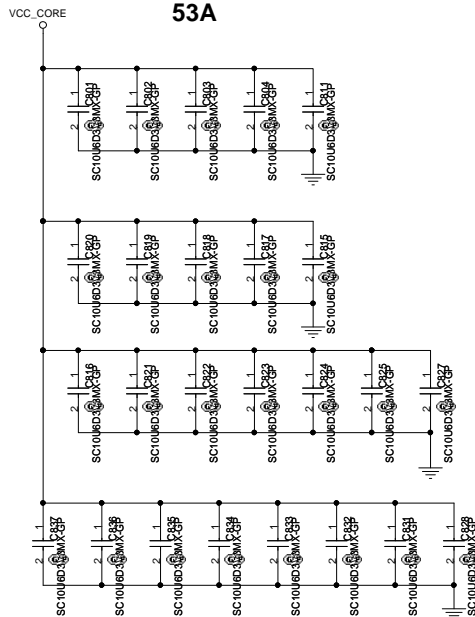
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SSID = CPU

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

POWER

CPU1F

6 OF 9

IVY-BRIDGE

PEG AND DDR

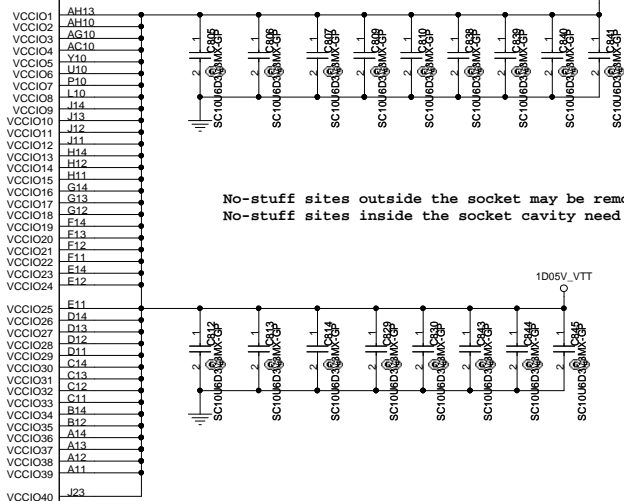
CORE SUPPLY

SVID

SENSE LINES

VCC1	AG35
VCC2	AG34
VCC3	AG33
VCC4	AG32
VCC5	AG31
VCC6	AG30
VCC7	AG29
VCC8	AG28
VCC9	AG27
VCC10	AG26
VCC11	AF34
VCC12	AF33
VCC13	AF32
VCC14	AF31
VCC15	AF30
VCC16	AF29
VCC17	AF28
VCC18	AF27
VCC19	AF26
VCC20	AD35
VCC21	AD34
VCC22	AD33
VCC23	AD32
VCC24	AD31
VCC25	AD30
VCC26	AD29
VCC27	AD28
VCC28	AD27
VCC29	AD26
VCC30	AC35
VCC31	AC34
VCC32	AC33
VCC33	AC32
VCC34	AC31
VCC35	AC30
VCC36	AC29
VCC37	AC28
VCC38	AC27
VCC39	AC26
VCC40	AA35
VCC41	AA34
VCC42	AA33
VCC43	AA32
VCC44	AA31
VCC45	AA30
VCC46	AA29
VCC47	AA28
VCC48	AA27
VCC49	AA26
VCC50	Y35
VCC51	Y34
VCC52	Y33
VCC53	Y32
VCC54	Y31
VCC55	Y30
VCC56	Y29
VCC57	Y28
VCC58	Y27
VCC59	Y26
VCC60	Y25
VCC61	V34
VCC62	V33
VCC63	V32
VCC64	V31
VCC65	V30
VCC66	V29
VCC67	V28
VCC68	V27
VCC69	V26
VCC70	V25
VCC71	U35
VCC72	U34
VCC73	U33
VCC74	U32
VCC75	U31
VCC76	U30
VCC77	U29
VCC78	U28
VCC79	U27
VCC80	U26
VCC81	R35
VCC82	R34
VCC83	R33
VCC84	R32
VCC85	R31
VCC86	R30
VCC87	R29
VCC88	R28
VCC89	R27
VCC90	R26
VCC91	P35
VCC92	P34
VCC93	P33
VCC94	P32
VCC95	P31
VCC96	P30
VCC97	P29
VCC98	P28
VCC99	P27
VCC100	P26

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

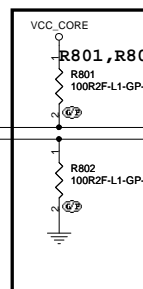
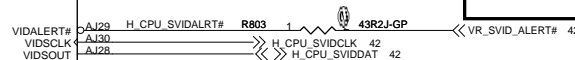


No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

close to CPU

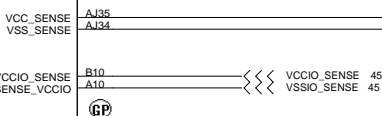
H CPU SVIDDATT R804 1 130R2F-1-GP

PR4201 PU



close to CPU

VCCSENSE 42
VSSSENSE 42



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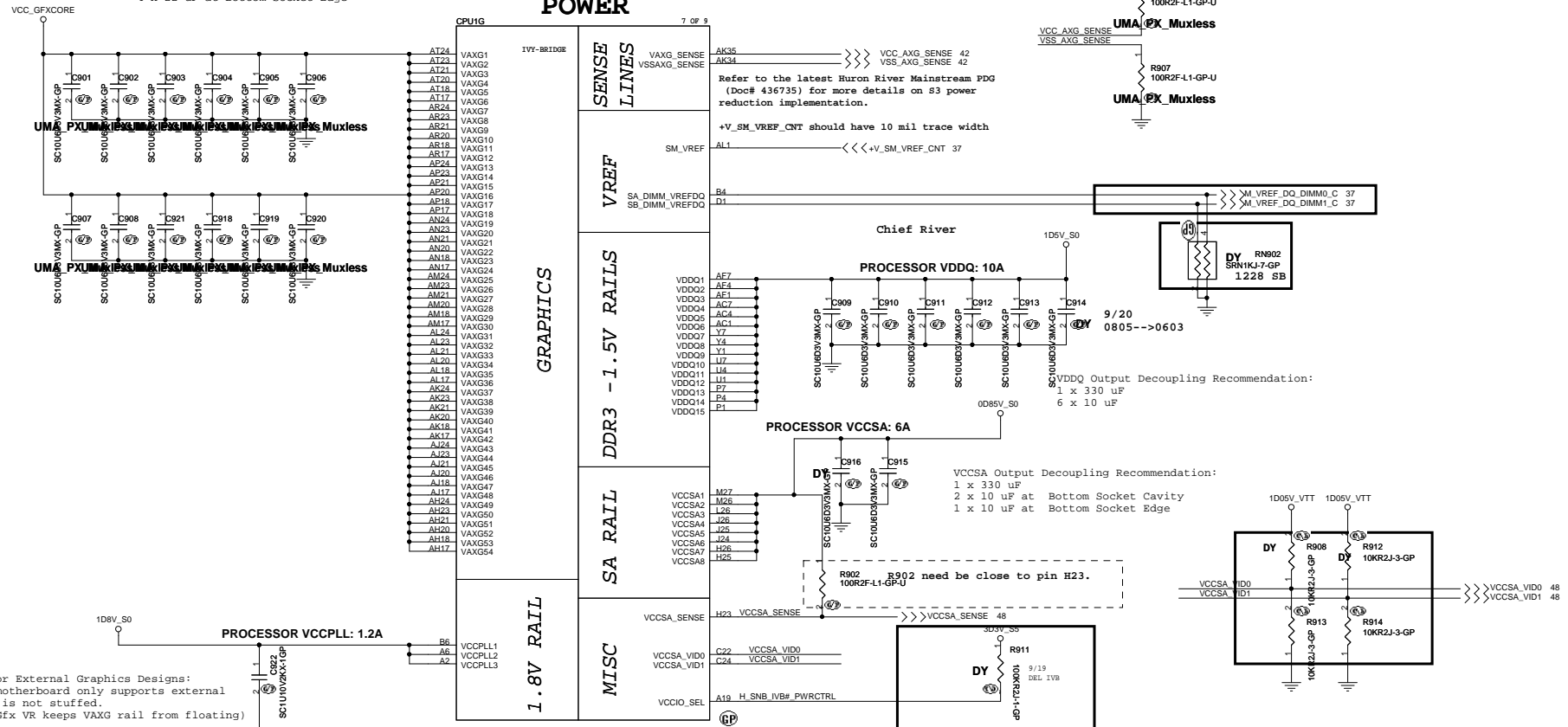
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SSID = CPU

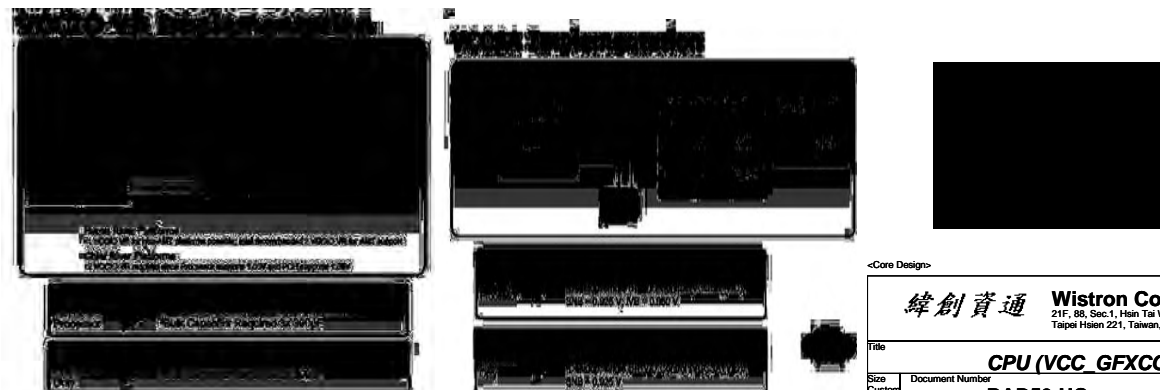
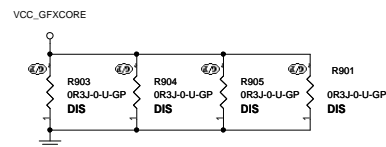
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VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge
```

R906,R907 close to CPU



Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

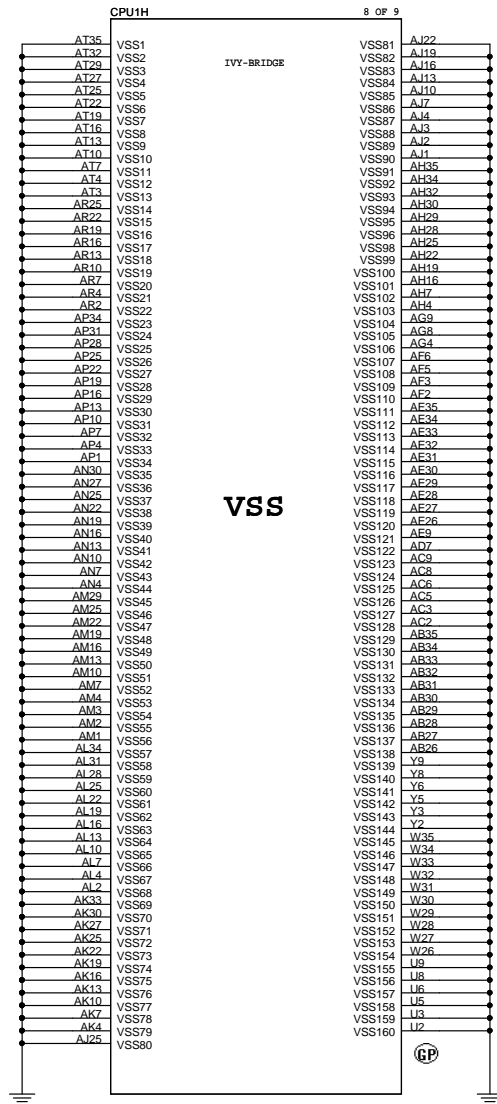


<Core Design:

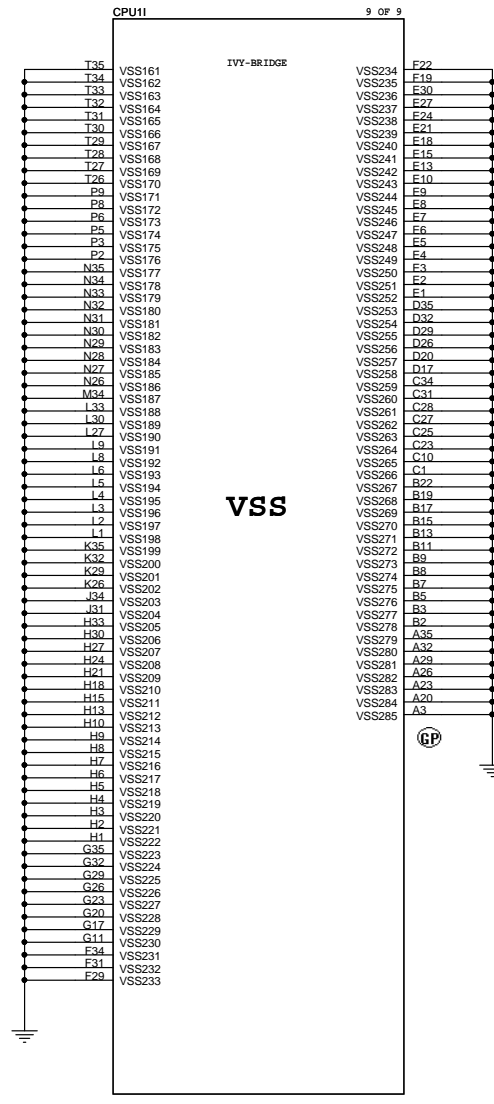
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (VCC_GFXCORE)			
Size	Document Number	Rev	
Custom	BAD50-HC	-1	
Date:	Thursday, March 29, 2012	Sheet 9 of	109

SSID = CPU



62.10055.321



62.10055.321

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

A3

Document Number

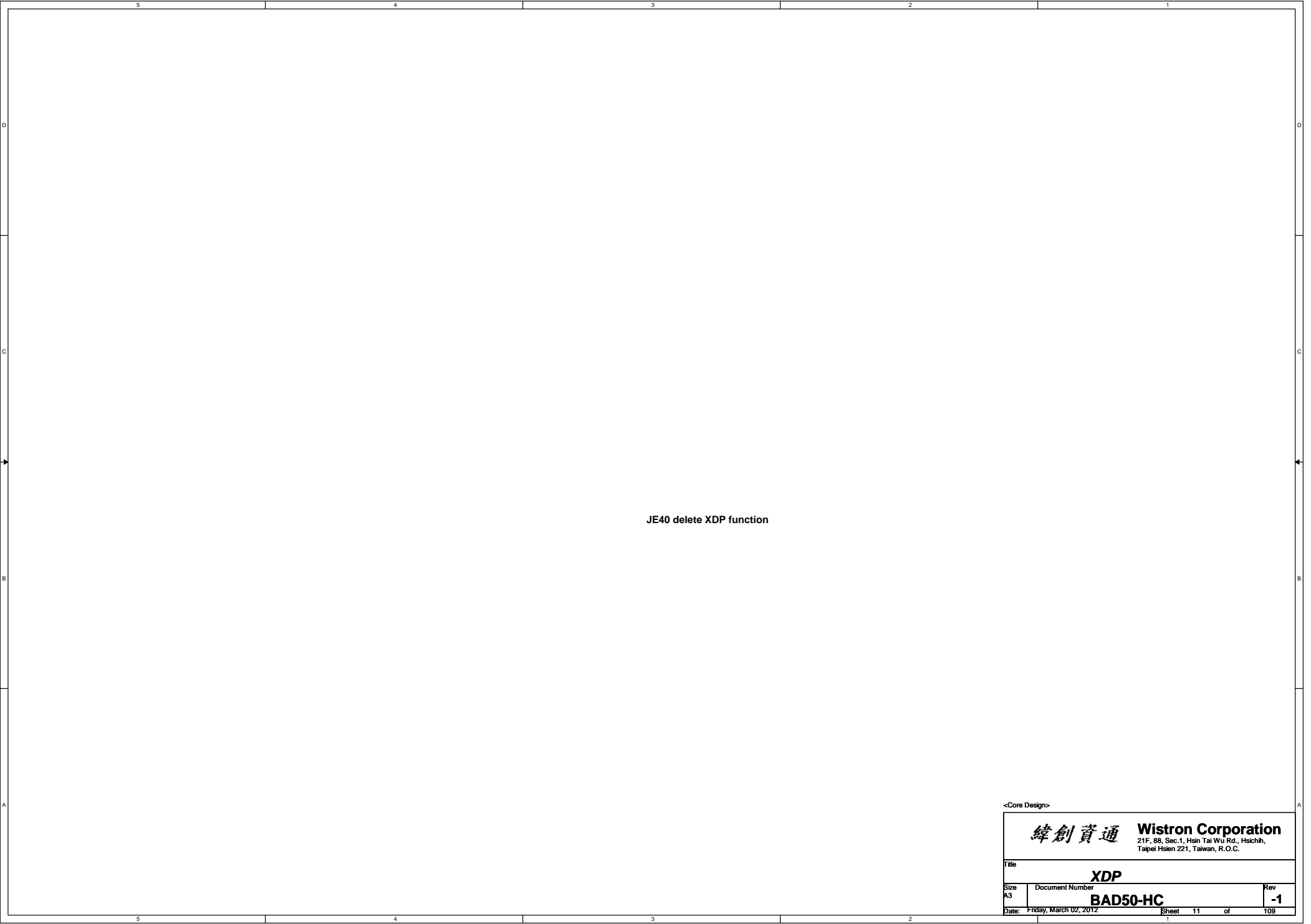
BAD50-HC

Rev

-1

Date: Friday, March 02, 2012

Sheet 10 of 109



JE40 delete XDP function

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
XDP			
Size	Document Number		Rev
A3	BAD50-HC		-1
Date:	Friday, March 02, 2012		Sheet 11 of 109

(Blanking)

<Core Design>

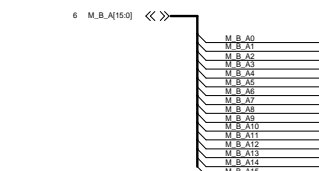
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 12 of 109

(Blanking)

<Core Design>

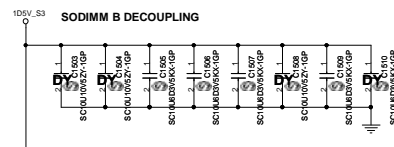
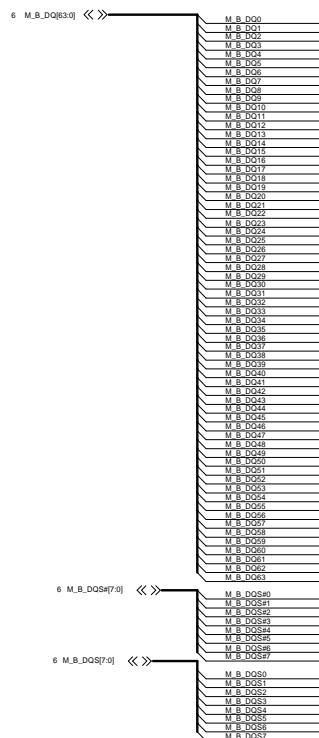
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 13 of 109

SSID = MEMORY

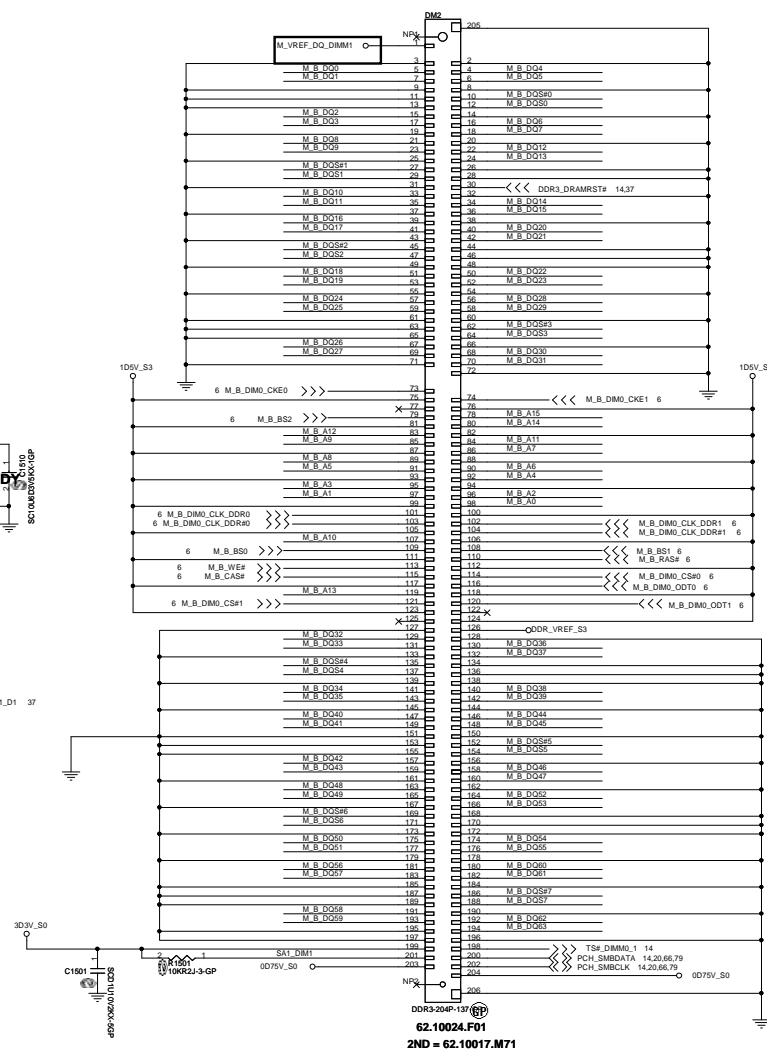
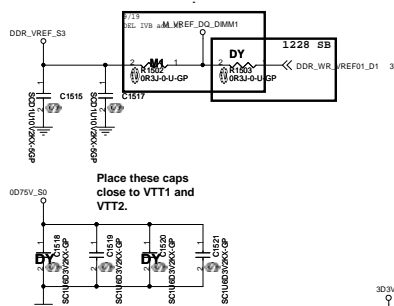


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



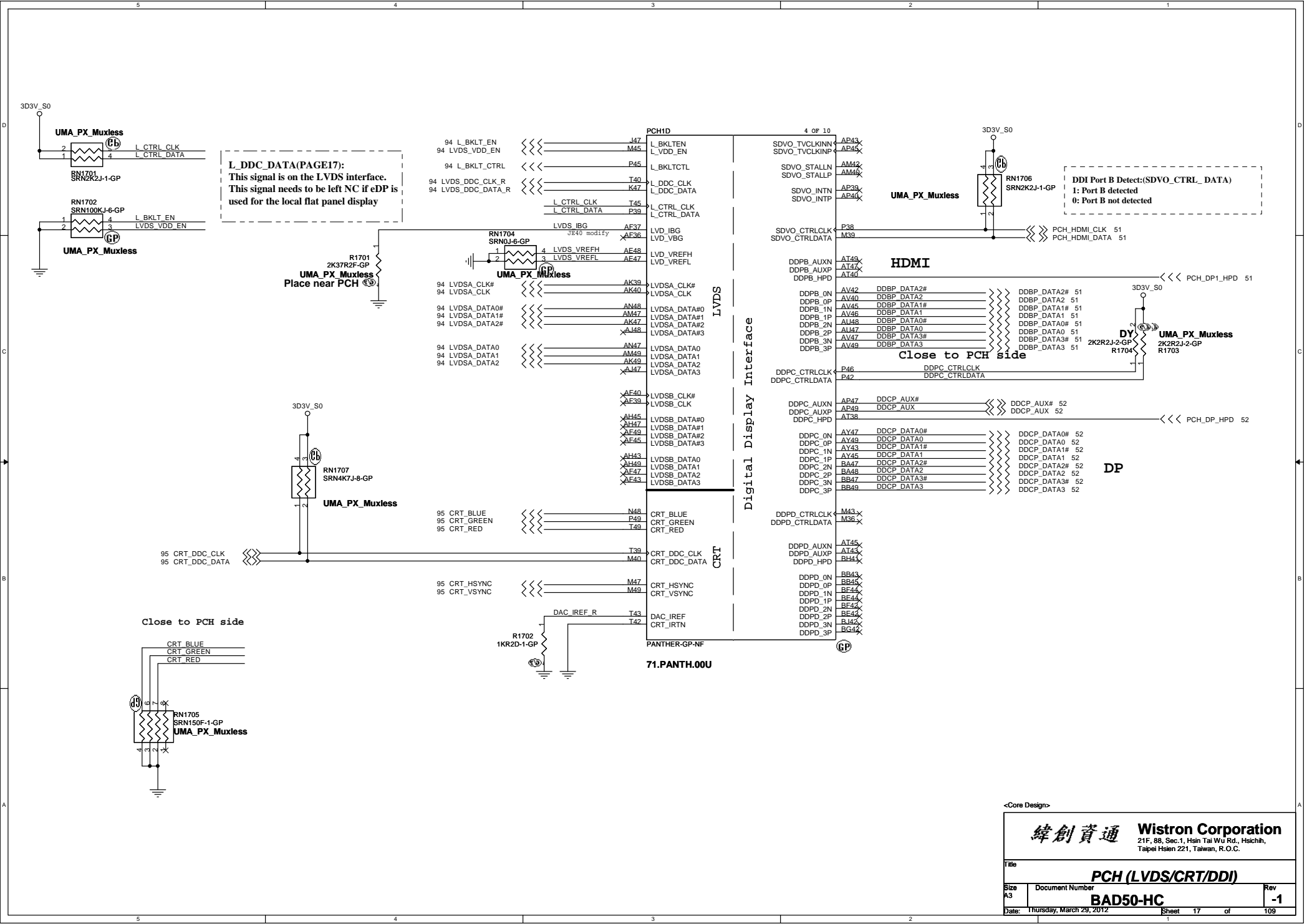
Layout Note:
Place these Caps near
SO-DIMMB.



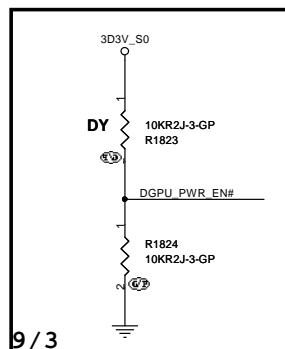
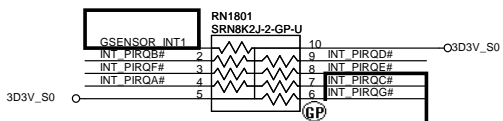
(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
DDR3-SODIMM2		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 16 of 109

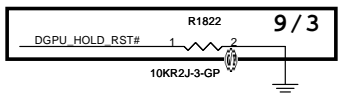


SSID = PCH



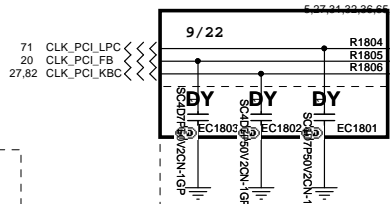
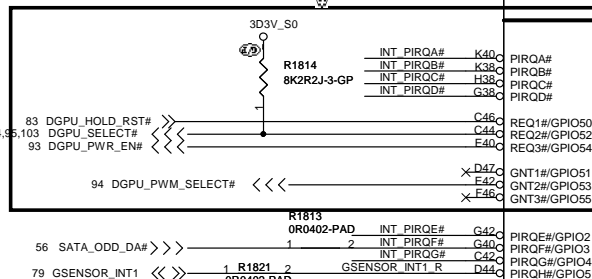
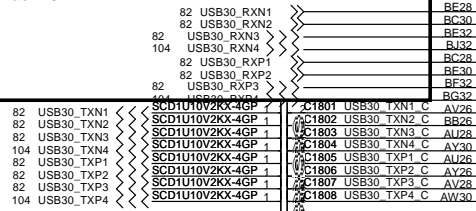
Al6 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT#3 Low = Al6 swap
override/Top-Block
Swap Override enabled
High = Default



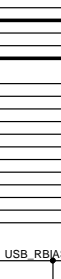
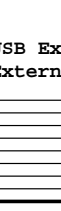
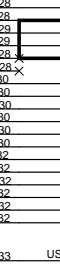
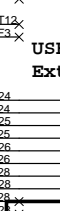
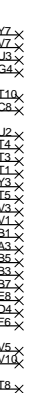
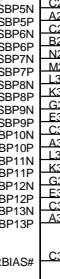
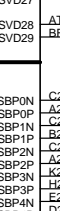
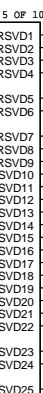
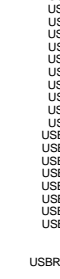
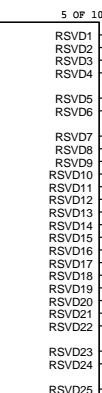
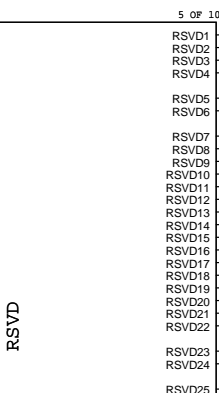
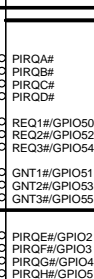
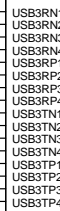
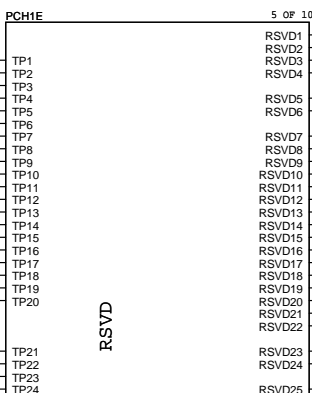
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

9/21 del USB REDRIVER

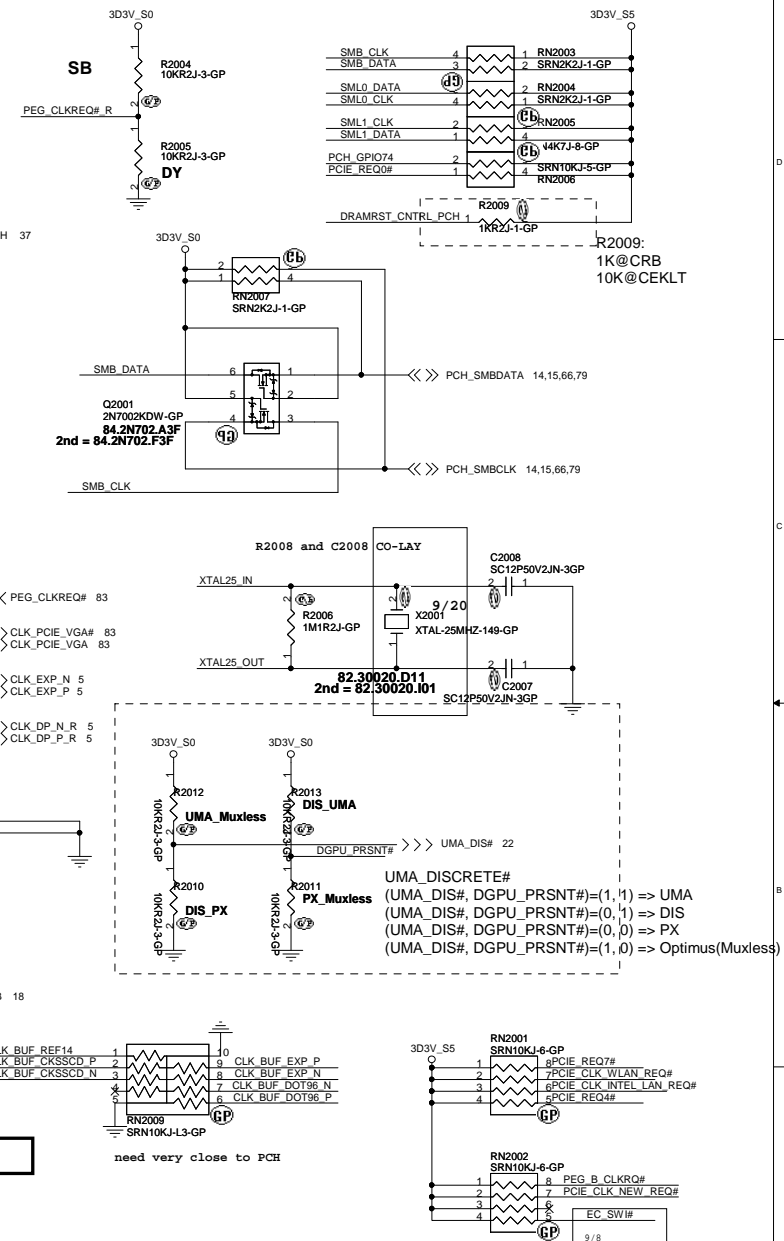
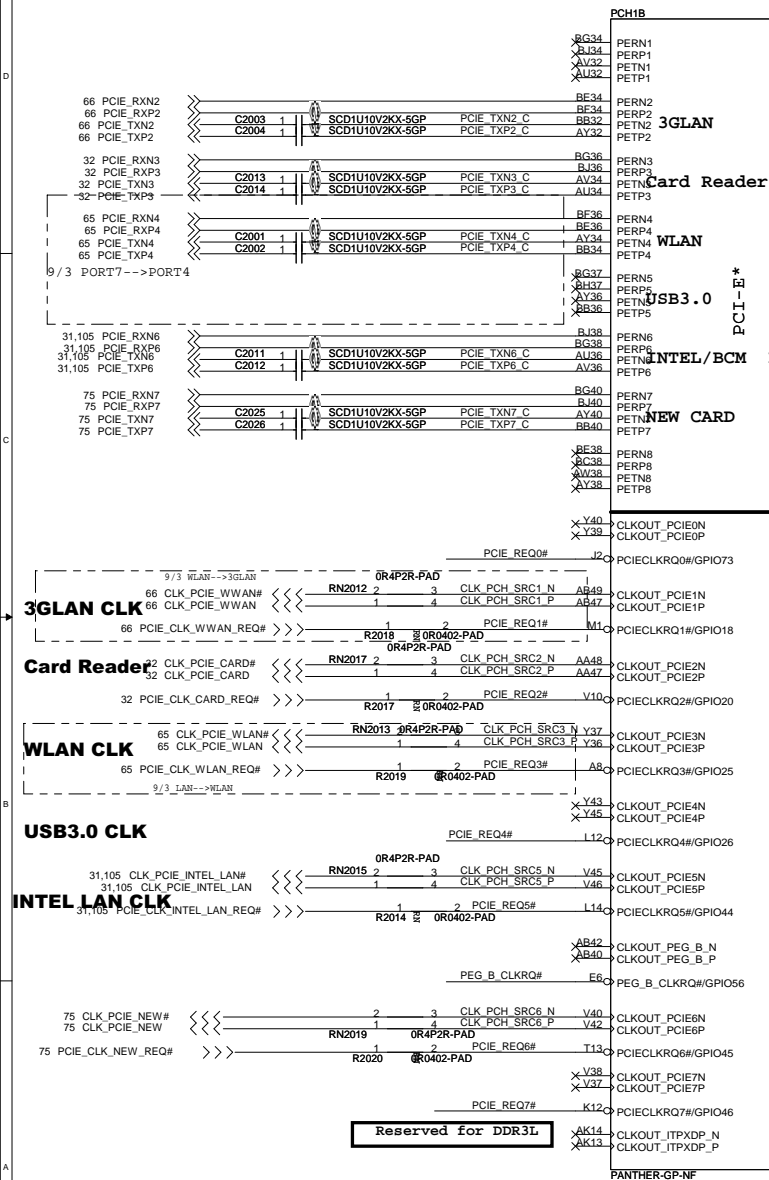


-1_0303

EMI request 20101109




SSID = PCH

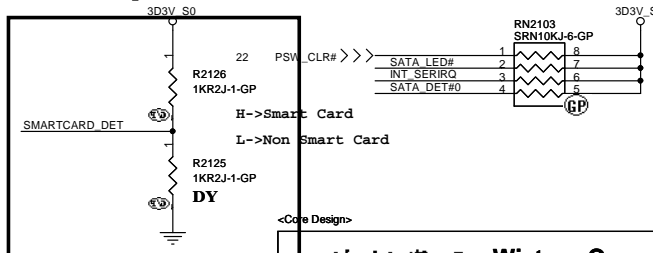
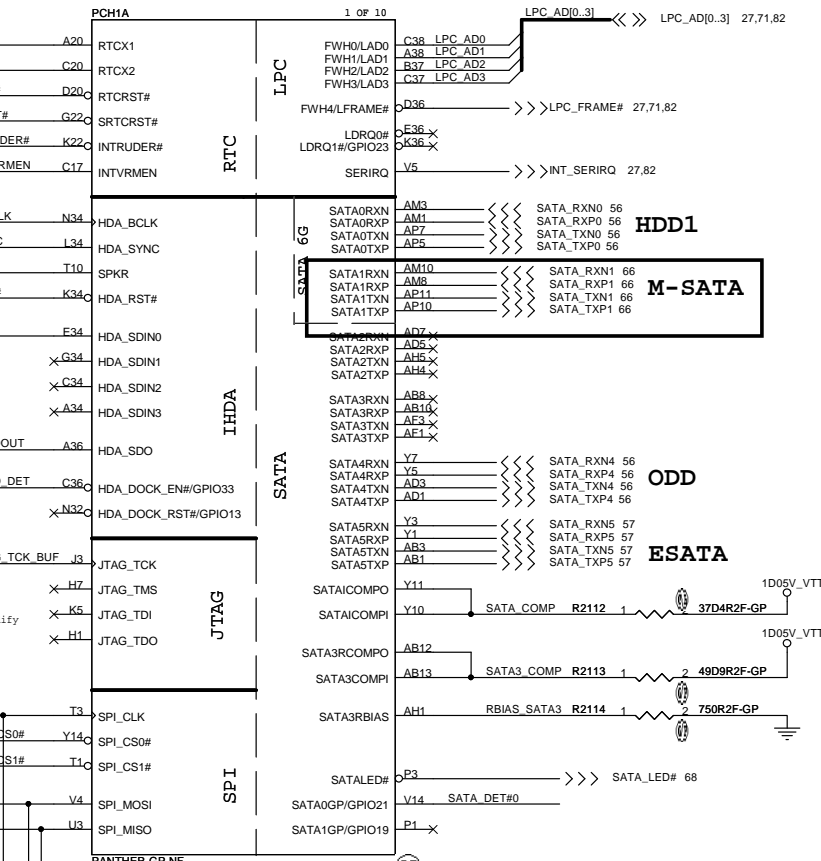
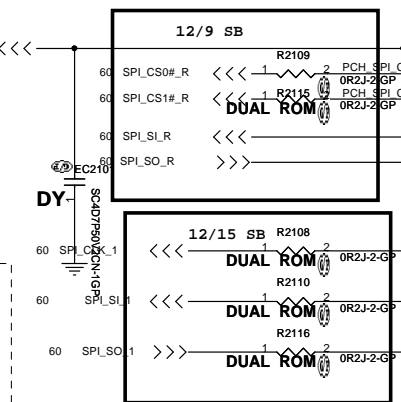
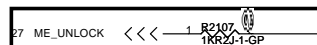
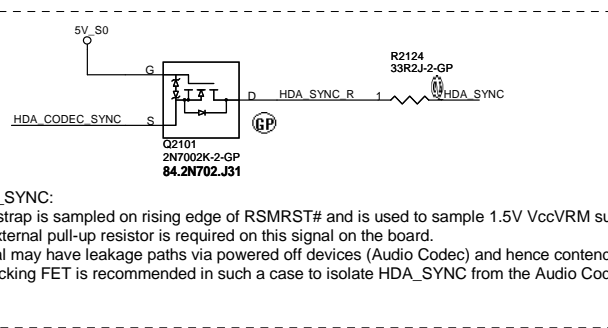
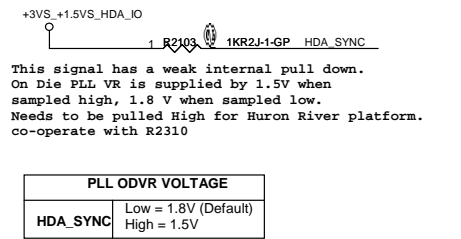
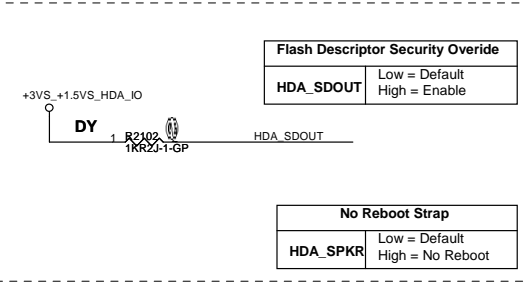
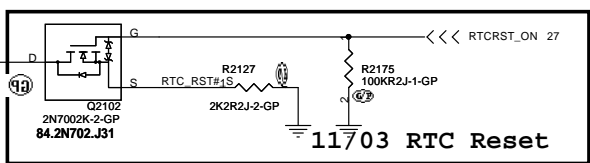
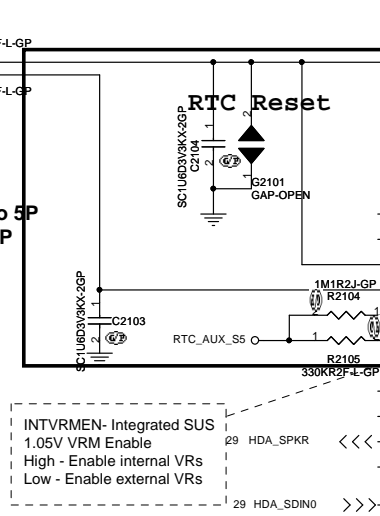
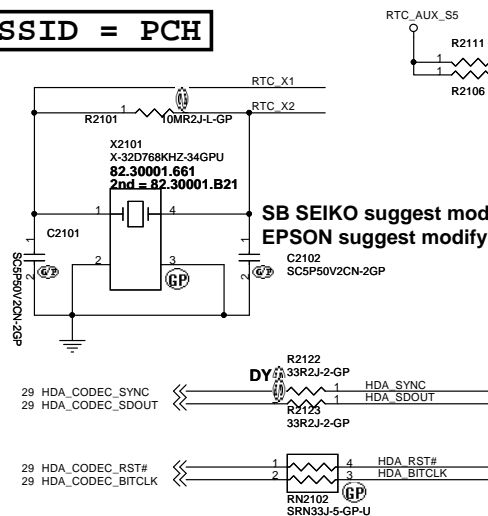


- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

<div> <div>  <div> 緯創資通 </div> </div> <div> <div> Wistron Corporation </div> <div> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipex Hsien 221, Taiwan, R.O.C. </div> </div> </div>			
Title			
PCH (PCI-E/SMBUS/CLOCK/CL)			
Size	Document Number	Rev	
Custom	BD50-HC	-1	
Date:	Thursday, March 29, 2012	Sheet	20 of 109

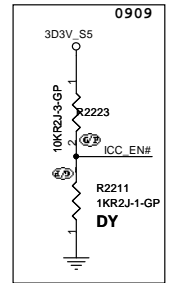
SSID = PCH



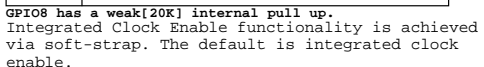
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size A3	Document Number		Rev
	BAD50-HC		-1
Date:	Saturday, March 03, 2012	Sheet 21 of	109

HDA₁_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.
1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

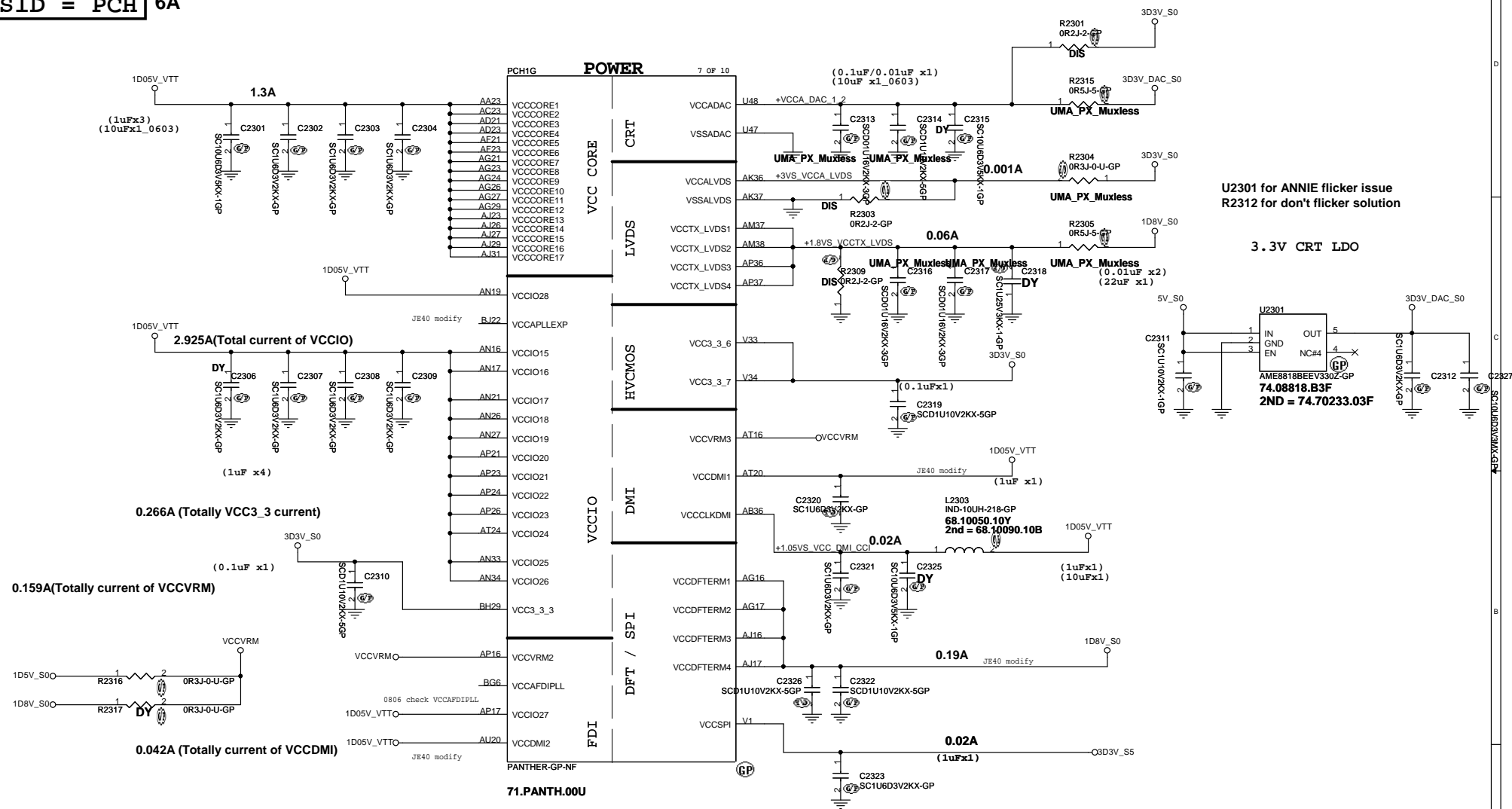


PLL_ODVR_EN 1 R2212 1KR2J-1-GP
DY



Title			
PCH (GPIO/CPU)			
Size A3	Document Number		Rev
	BAD50-HC		-1
Date:	Saturday, March 03, 2012	Sheet 22 of	109

SSID = PCH 6A



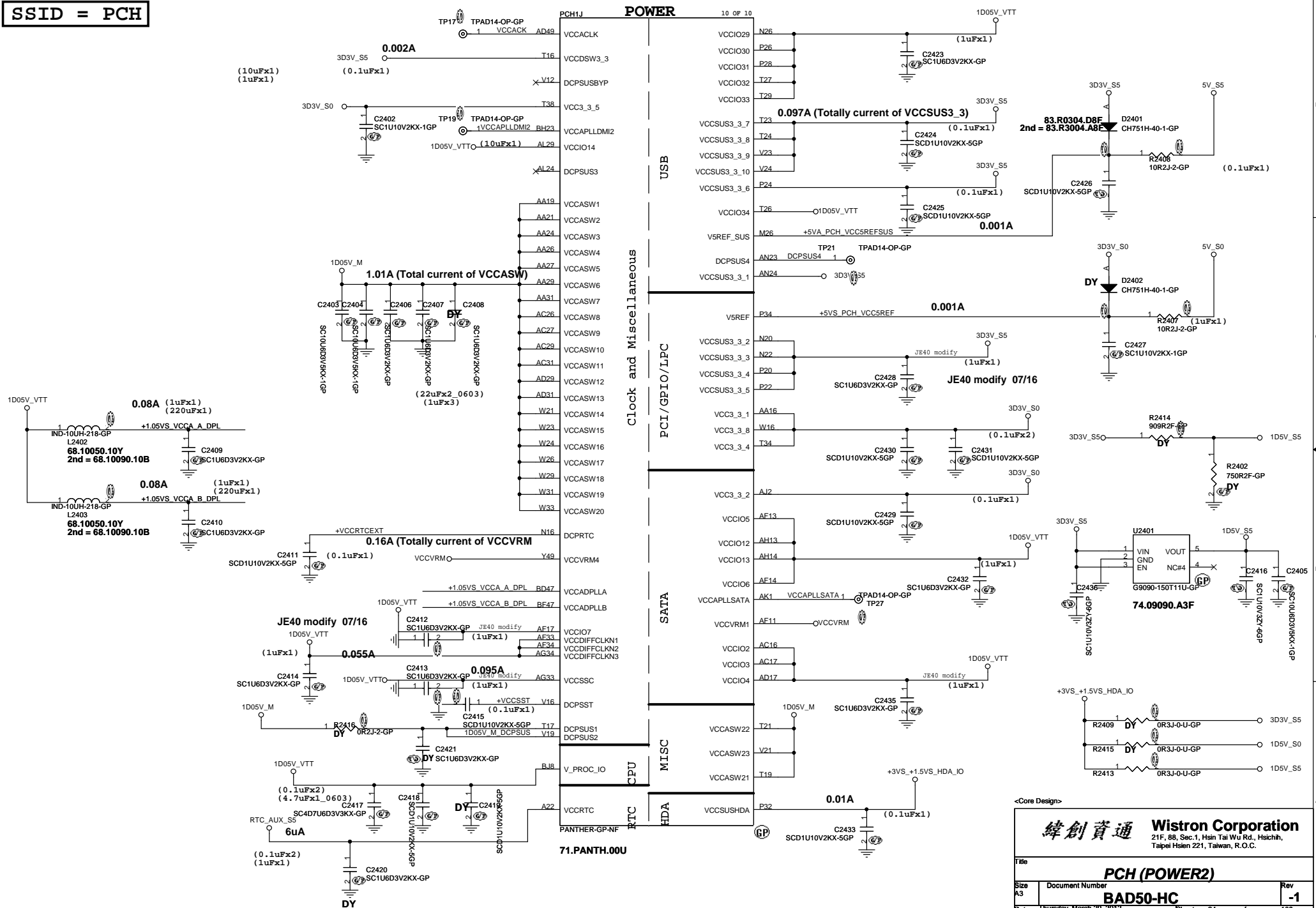
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

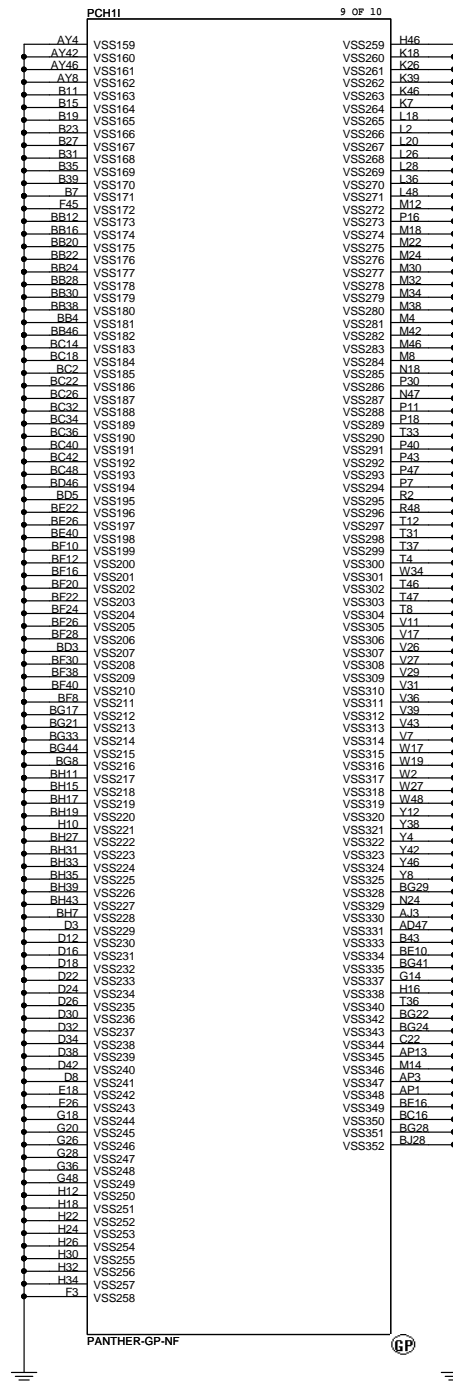
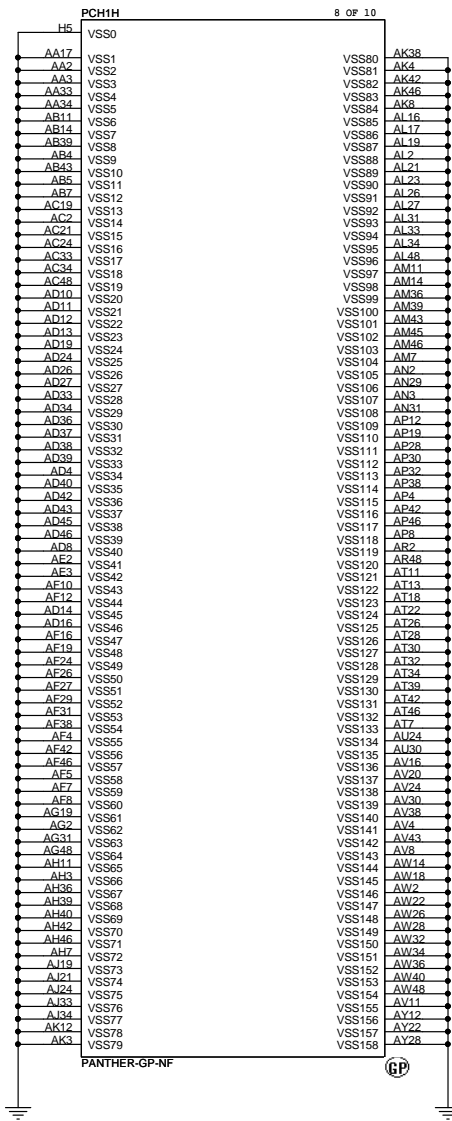
Title	PCH (POWER1)
-------	---------------------

Size A3	Document Number BAD50-HC	Rev -1
Date: Thursday, March 29, 2012	Sheet 23	of 109

SSID = PCH



SSID = PCH



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (VSS)

Size

Document Number

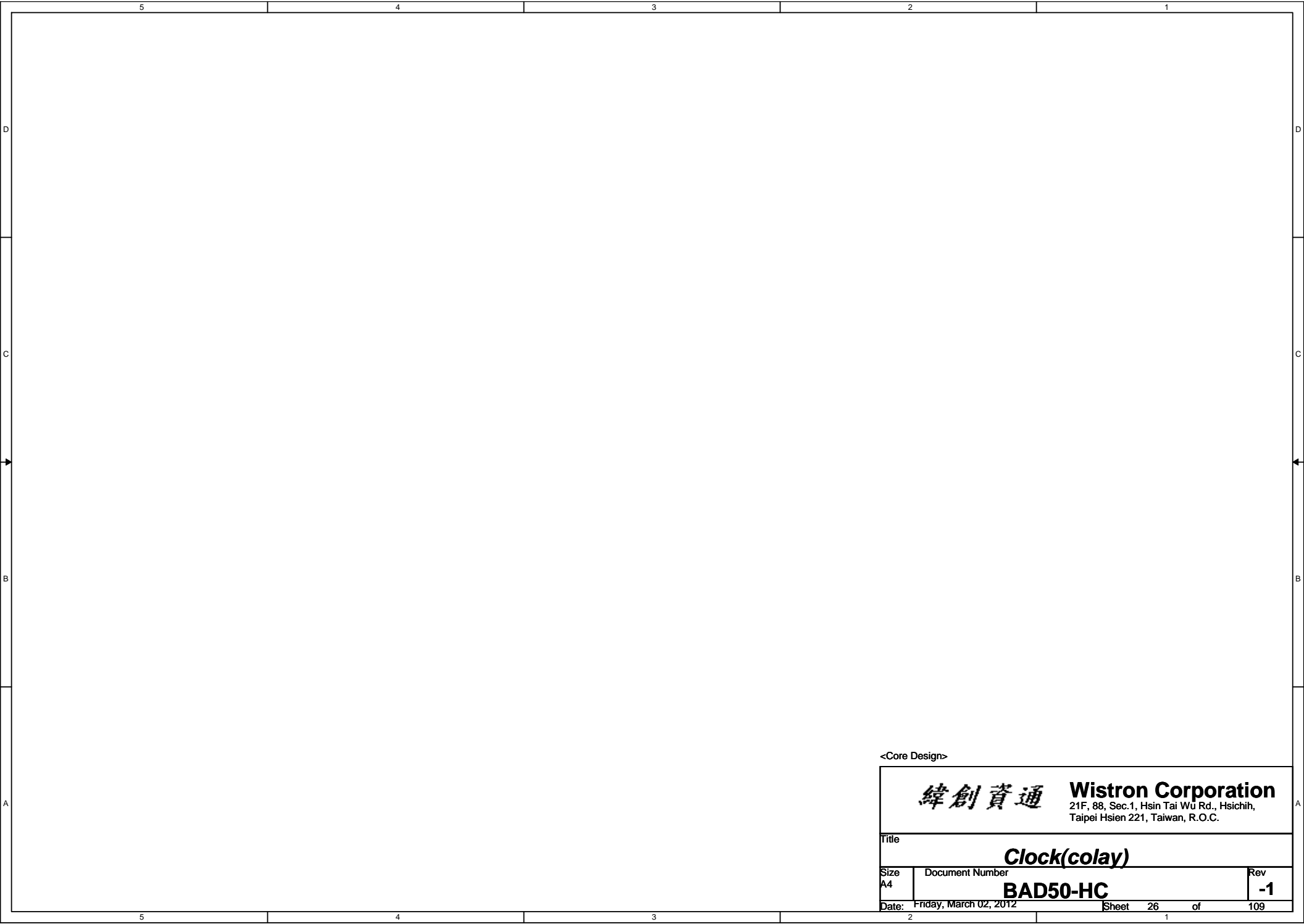
BAD50-HC

Rev

-1

Date: Friday, March 02, 2012

Sheet 25 of 109

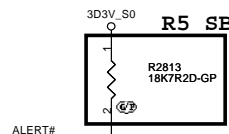
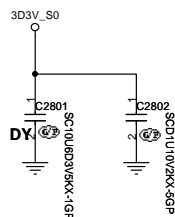


<Core Design>

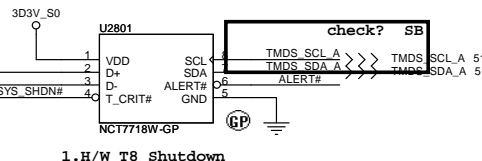
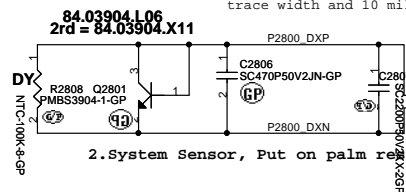
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title <div>Clock(colay)</div>	
Size <div>A4</div>	Rev <div>-1</div>
Date <div>Friday, March 02, 2012</div>	Sheet 26 of 109



SSID = Thermal



Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



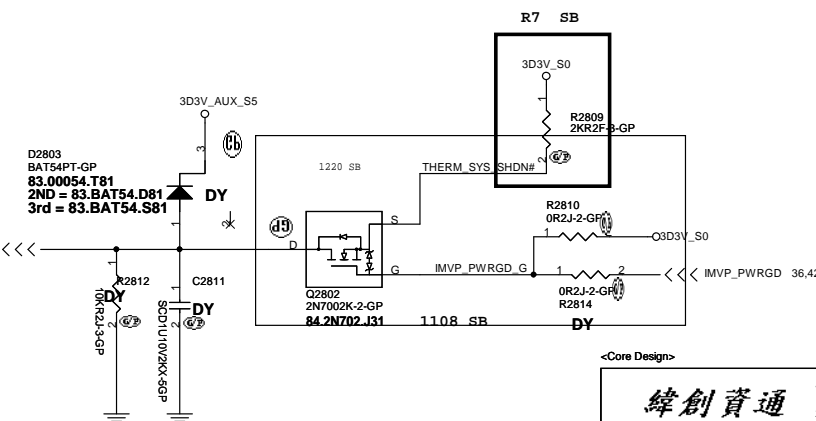
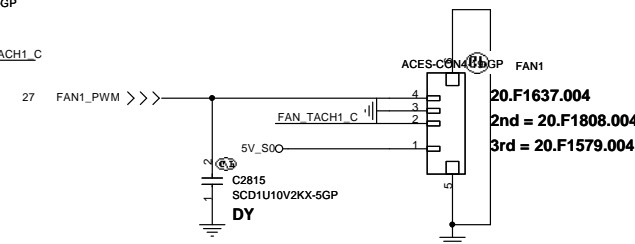
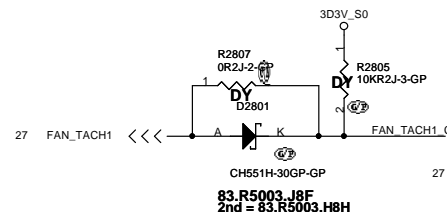
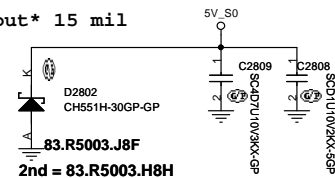
ALERT# /T CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

Fan controller P2793

Layout 15 mil



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

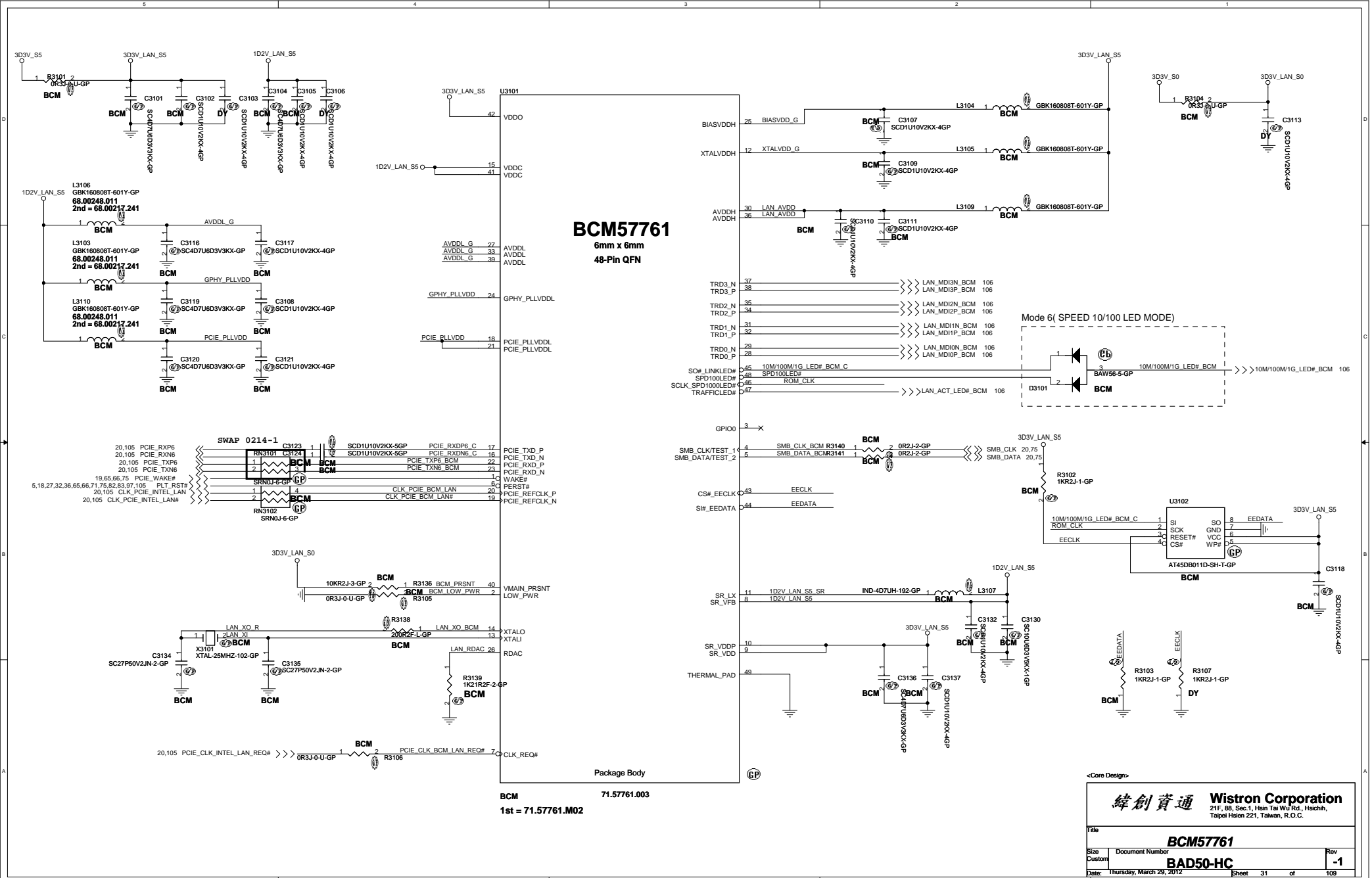
Title Thermal NCT7718W/Fan
Size Custom Document Number BAD50-HC
Date: Thursday, March 29, 2012 Sheet 28 of 109

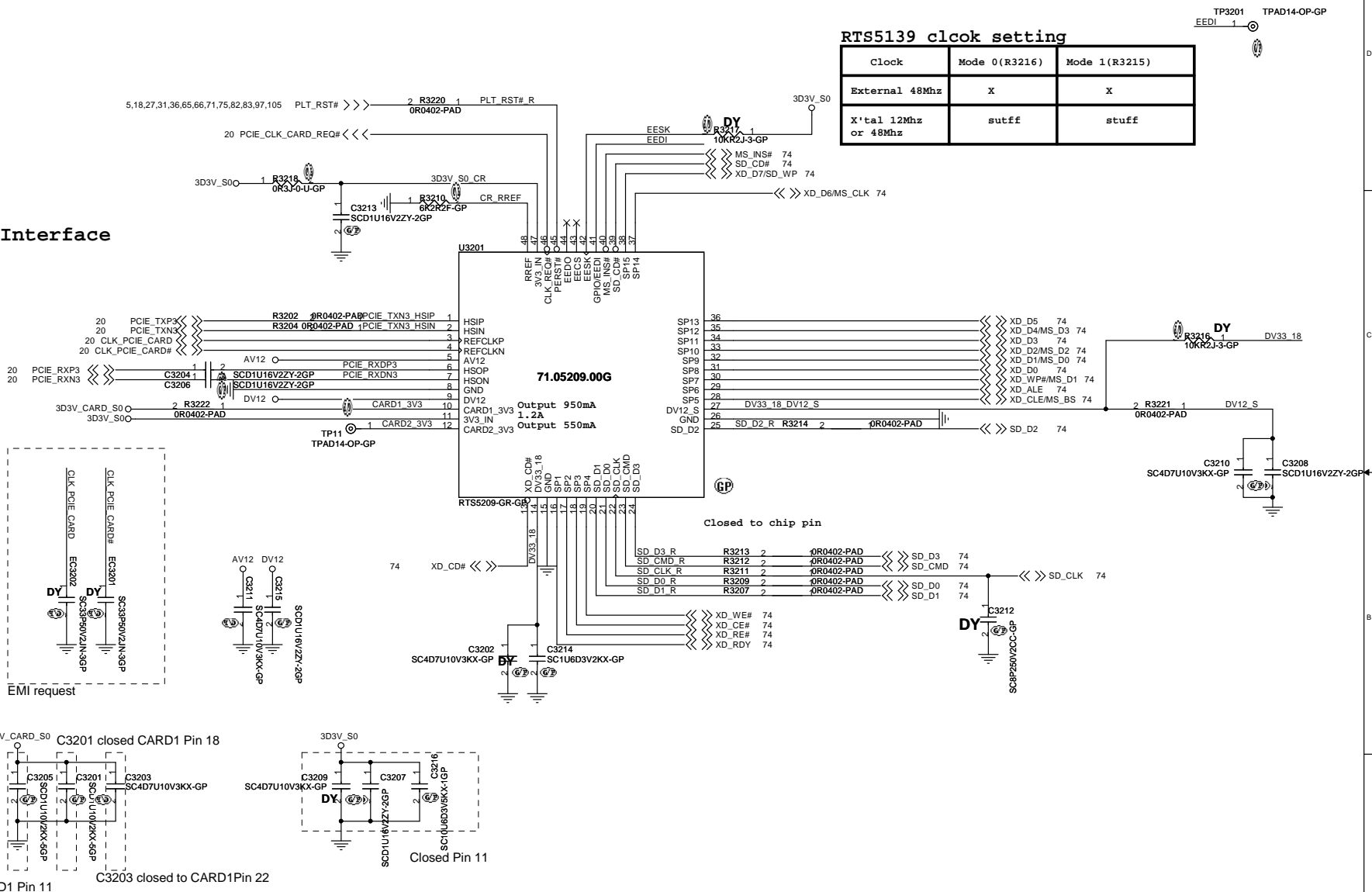
AUDIO OP AMPLIFIER

JE40 delete AMP function

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Audio AMP		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 30 of 109

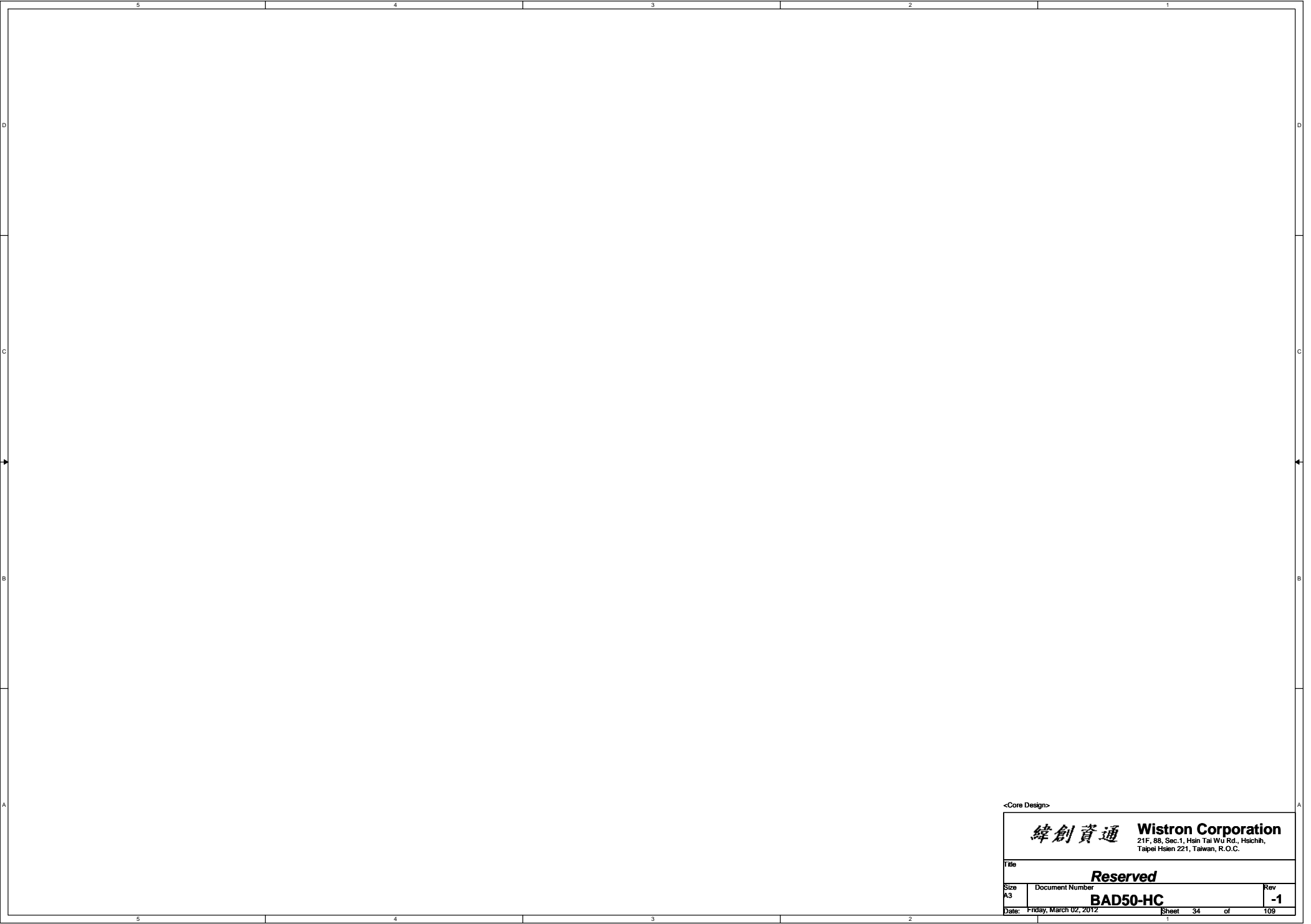




(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date: Friday, March 02, 2012		Sheet 33 of 109

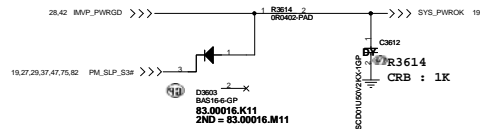


<Core Design>

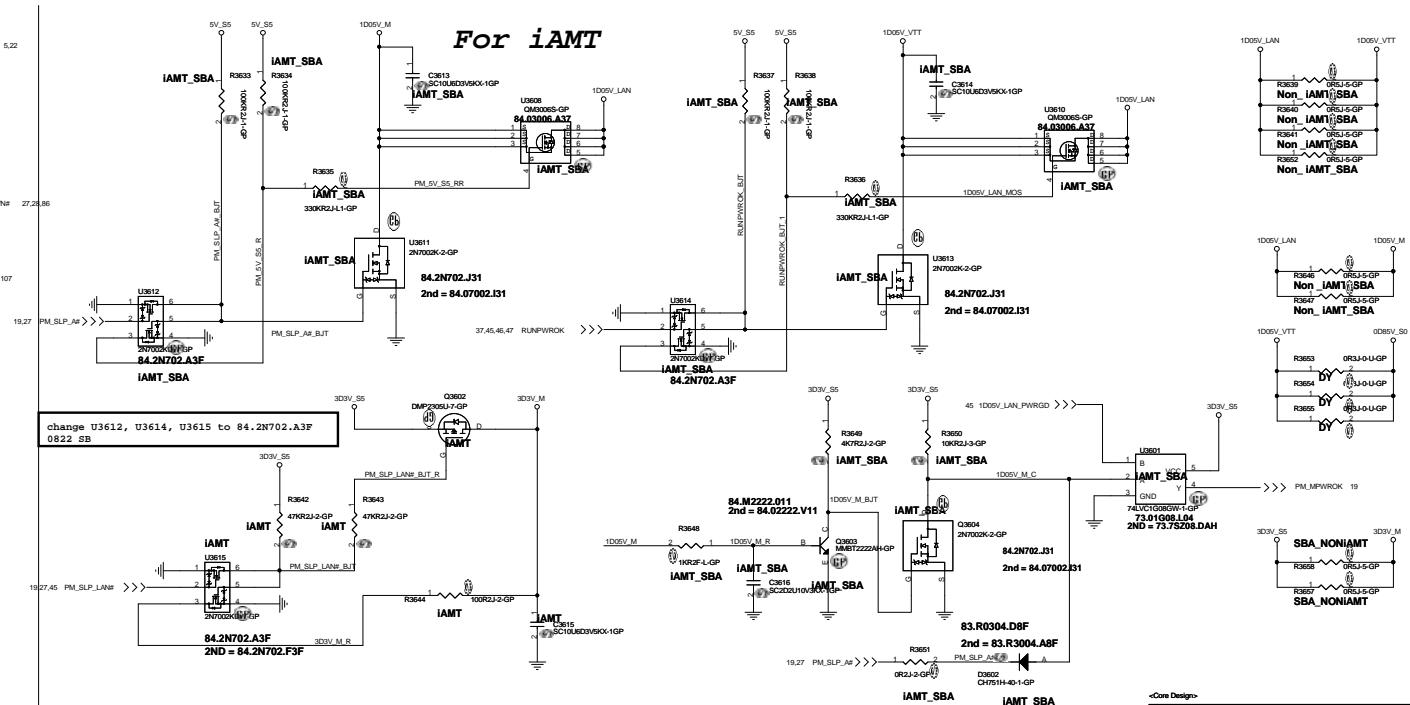
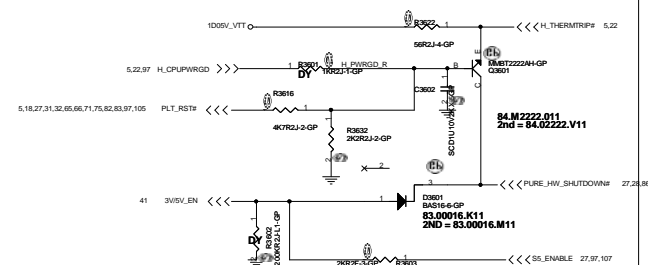
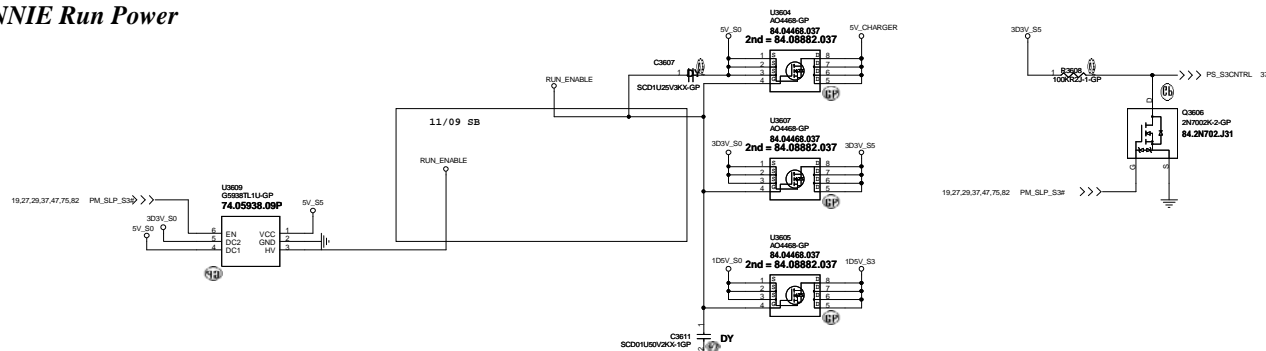
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A3	BAD50-HC		-1
Date:	Friday, March 02, 2012		Sheet 34 of 109

reserve

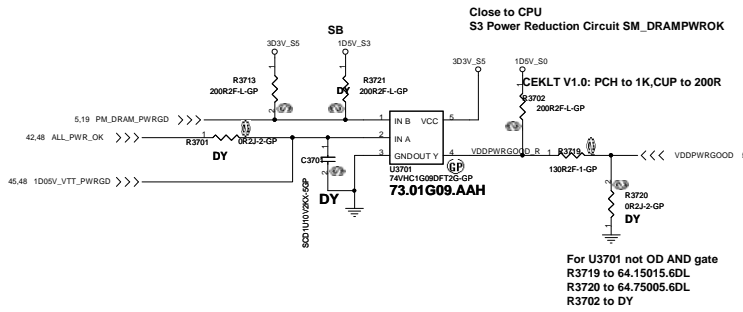
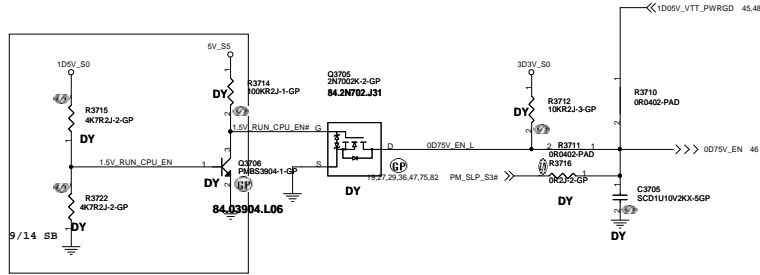
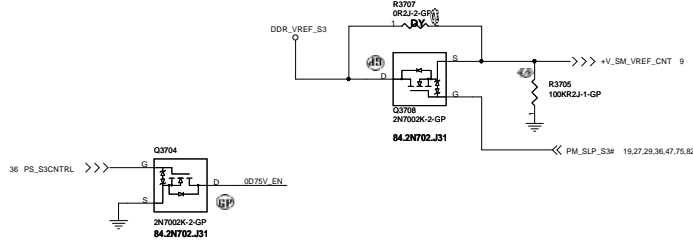
Power Sequence



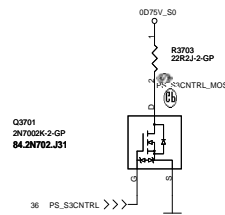
ANNIE Run Power



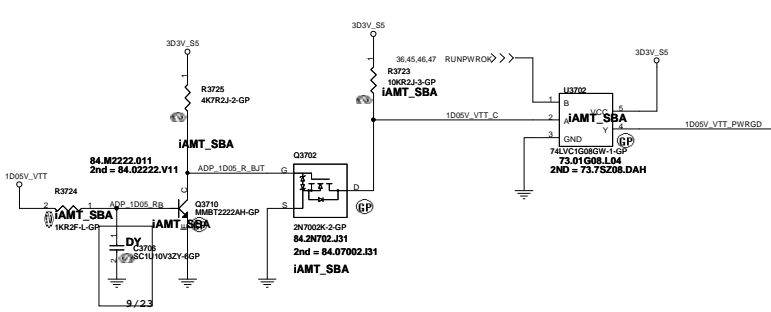
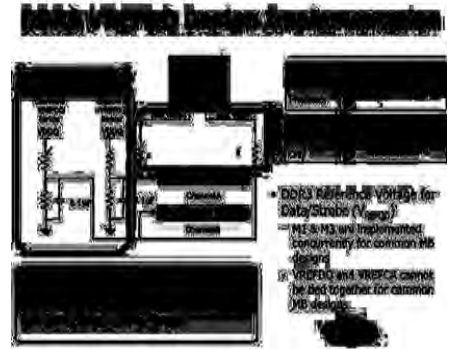
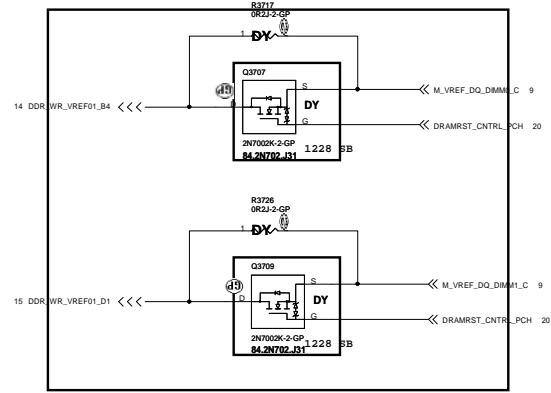
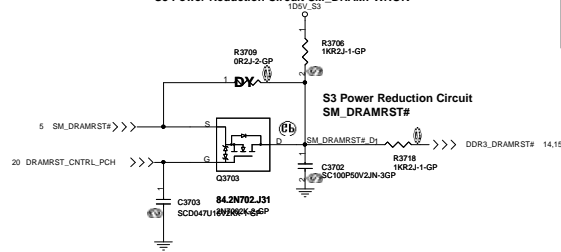
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



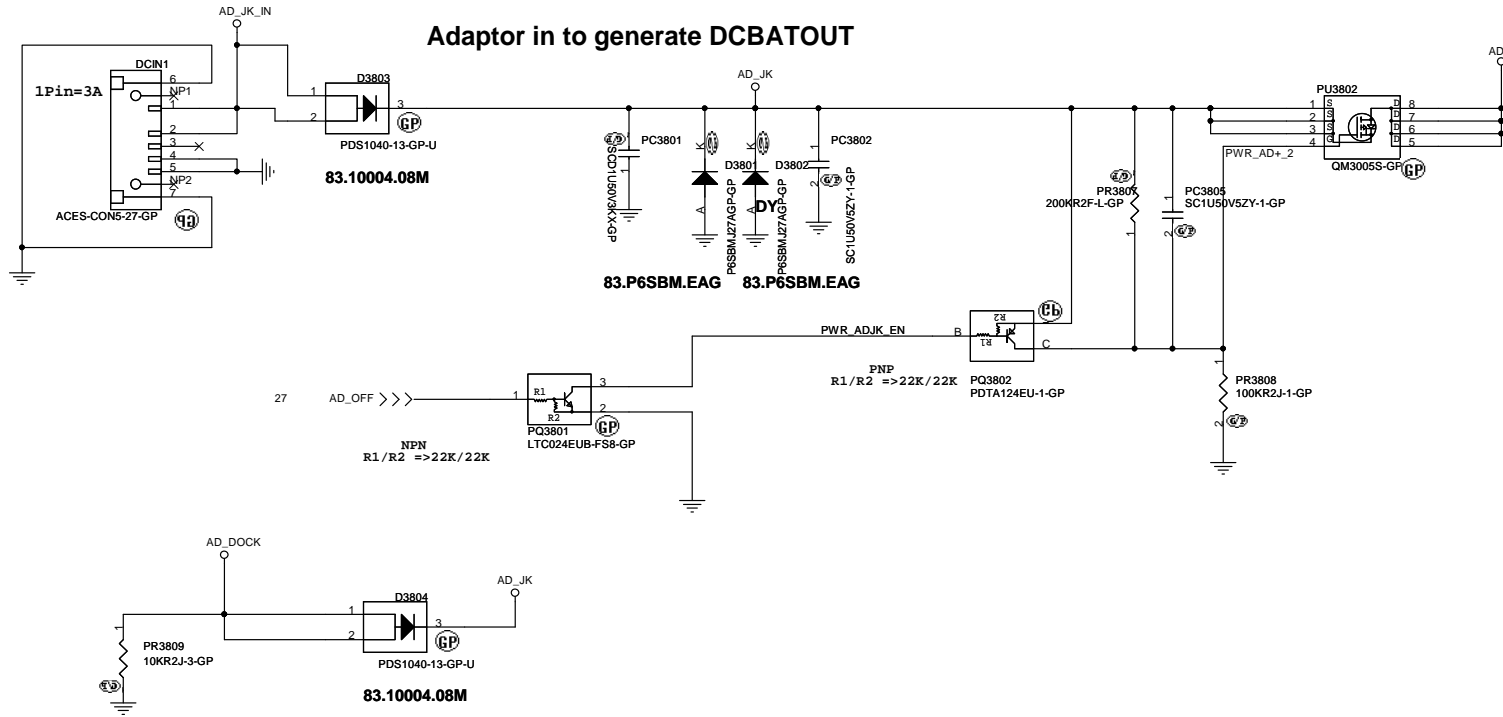
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



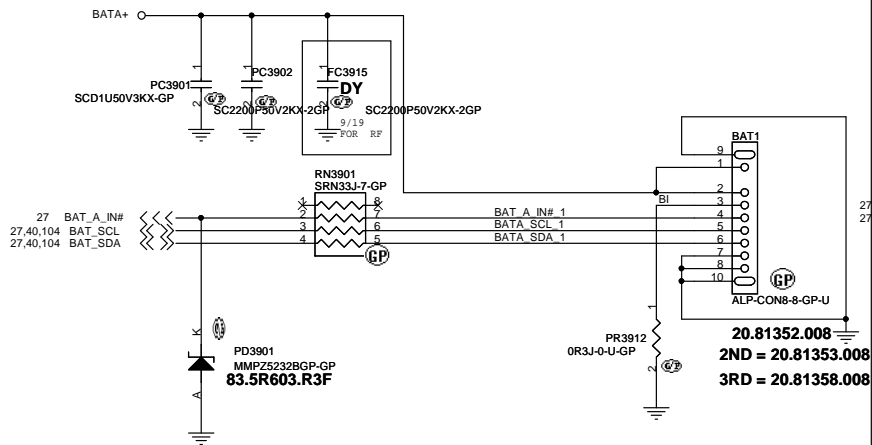
<Core Design>

ANNIE solution

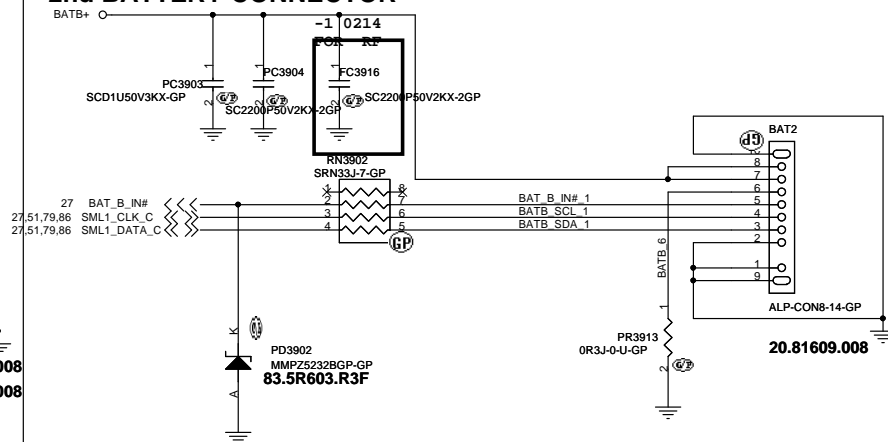
Adaptor in to generate DCBATOUT



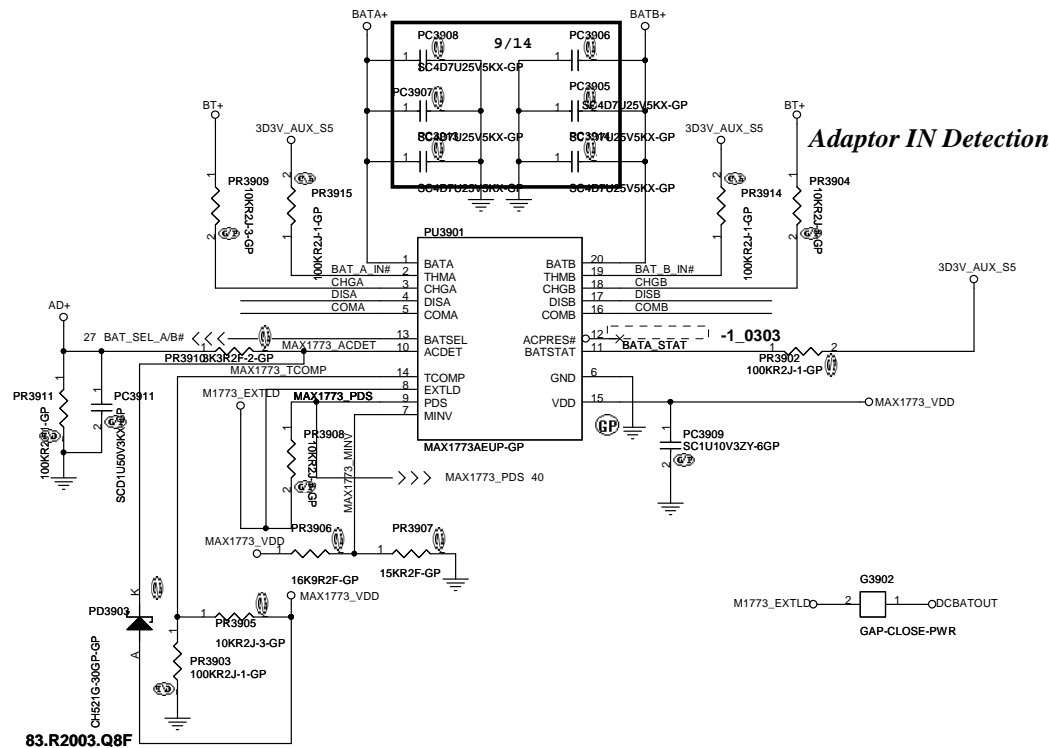
MAIN BATTERY CONNECTOR



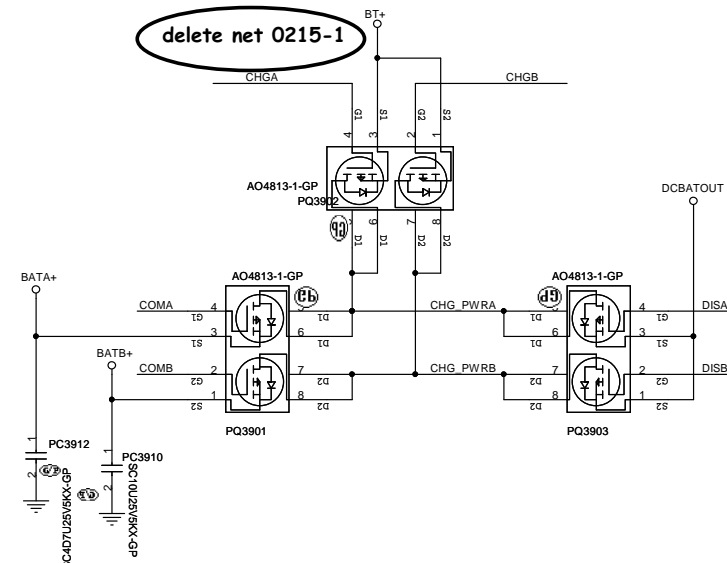
2nd BATTERY CONNECTOR



BATTERY SWITCH



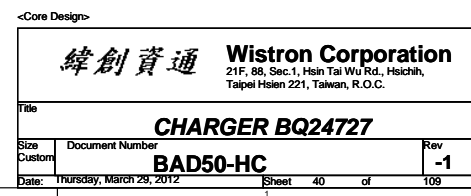
delete net 0215-1

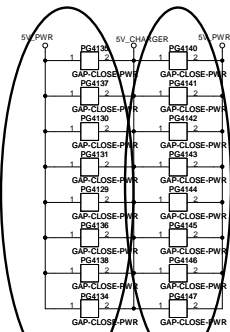
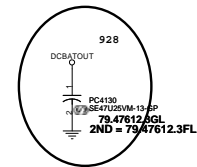


<Core Design>

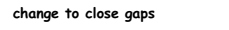
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			BATT CONN
Size	Document Number	Rev	
A3		BAD50-HC	
Date:	Thursday, March 29, 2012	Sheet	39 of 109

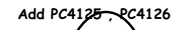




change to close gaps 1129



Iomax=6.5A
OCP>9.75A



change design current

$I_{\text{omax}}=15\text{A}$
 $\text{OCP}>21\text{A}$

change choke

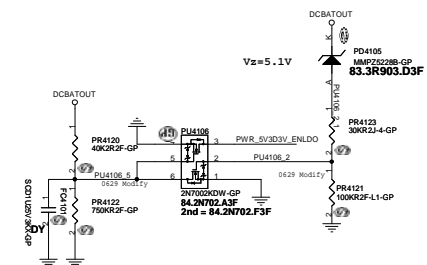
I_{omax}=15A
OCP>21A

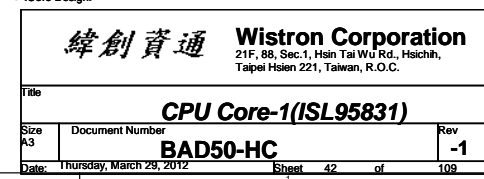
change choke

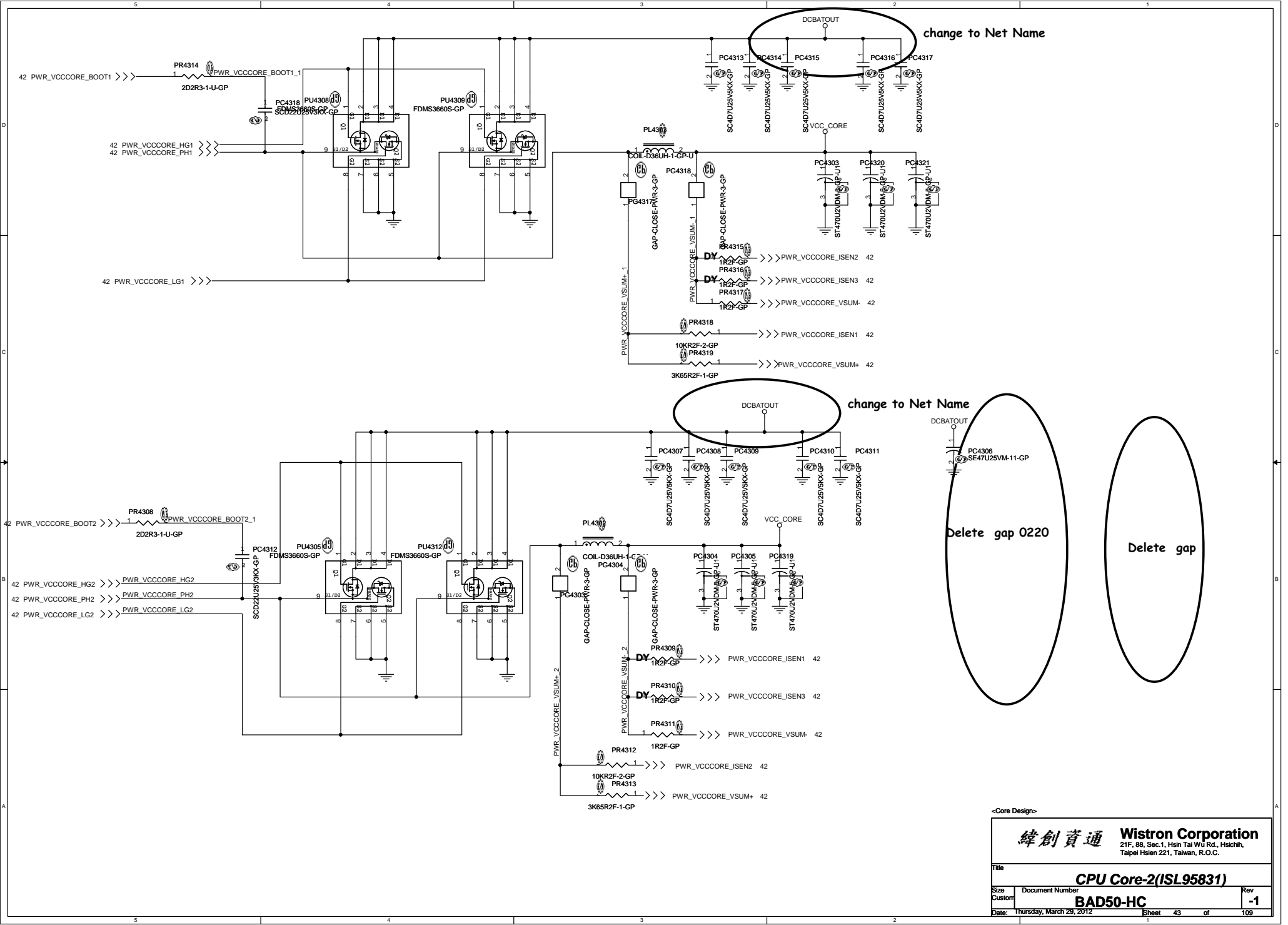
add ~~PC4103~~

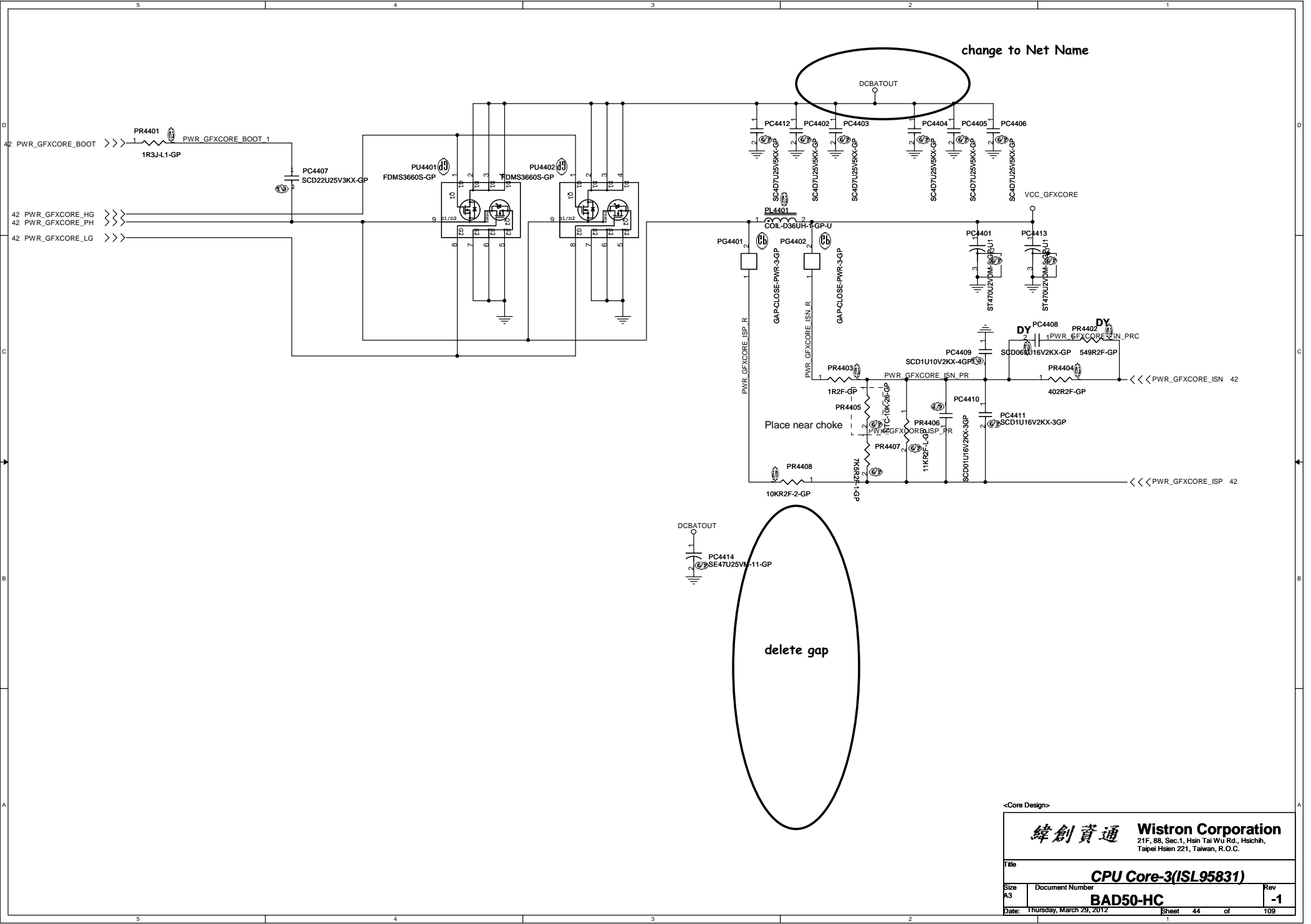
Set in 5V

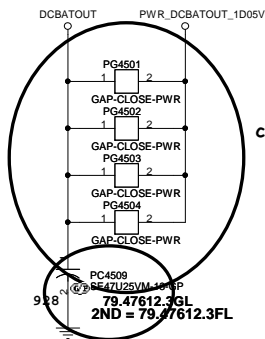
$$V_{out} = 2 * (1 + PR4113 / PR4117)$$





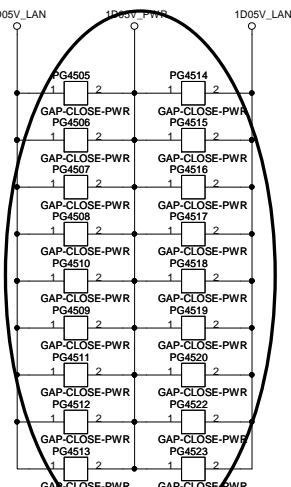
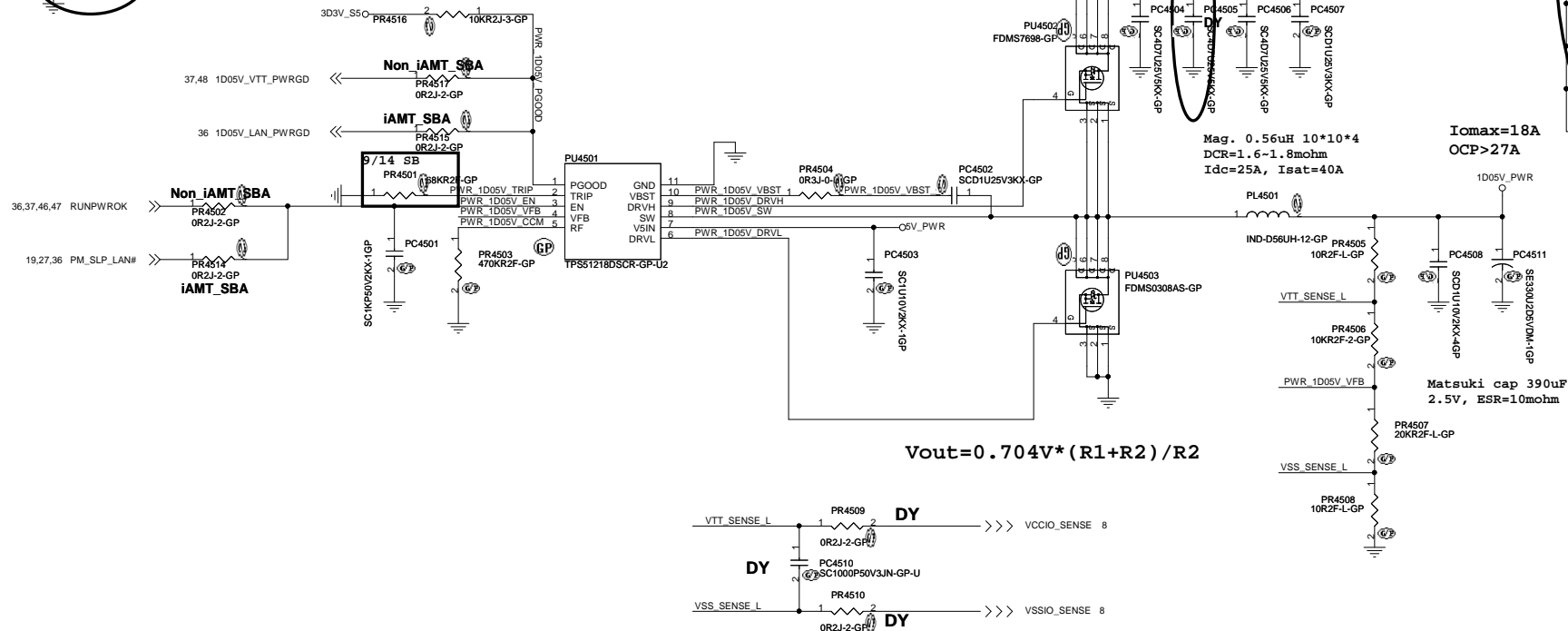






change to close gaps1129

TPS51218 for 1D05V



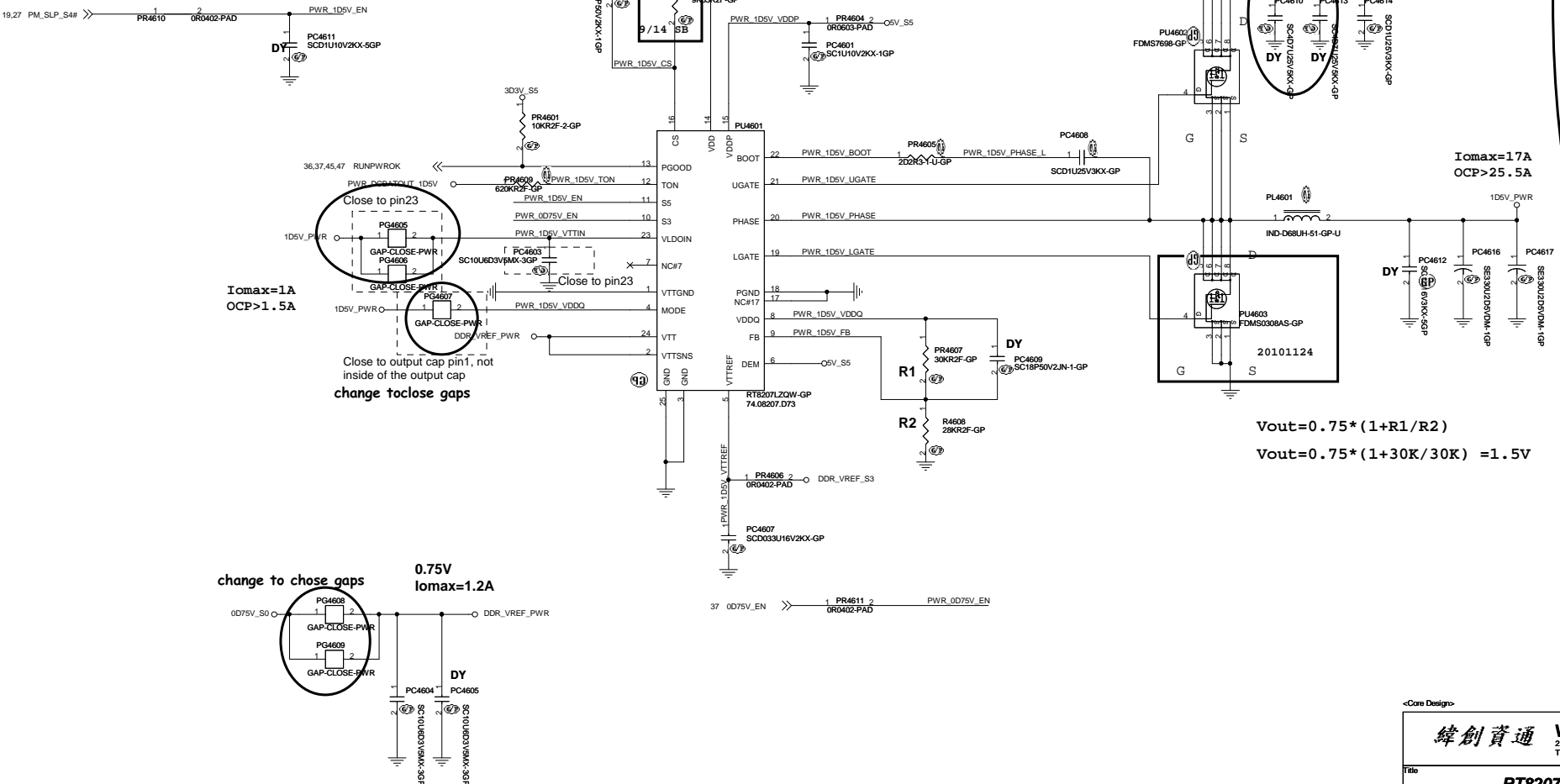
change to close gaps1129

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			
DC to DC 1D05V(TPS51218D)			
Size	Document Number	Rev	
Custom	BAD50-HC	-1	
Date:	Thursday, March 29, 2012	Sheet	45 of 109

RT8207L for 1D5V

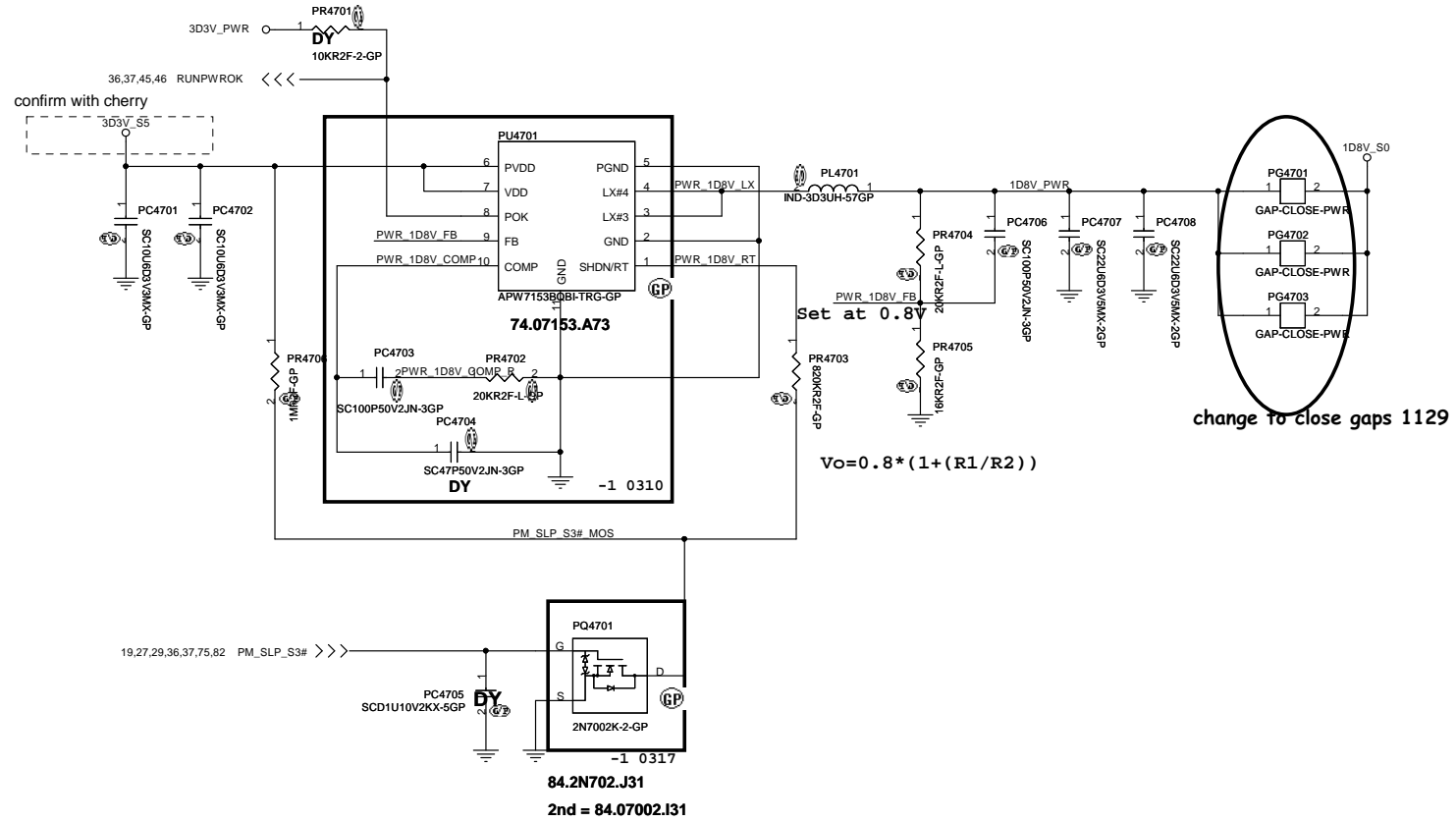


<Core Design>

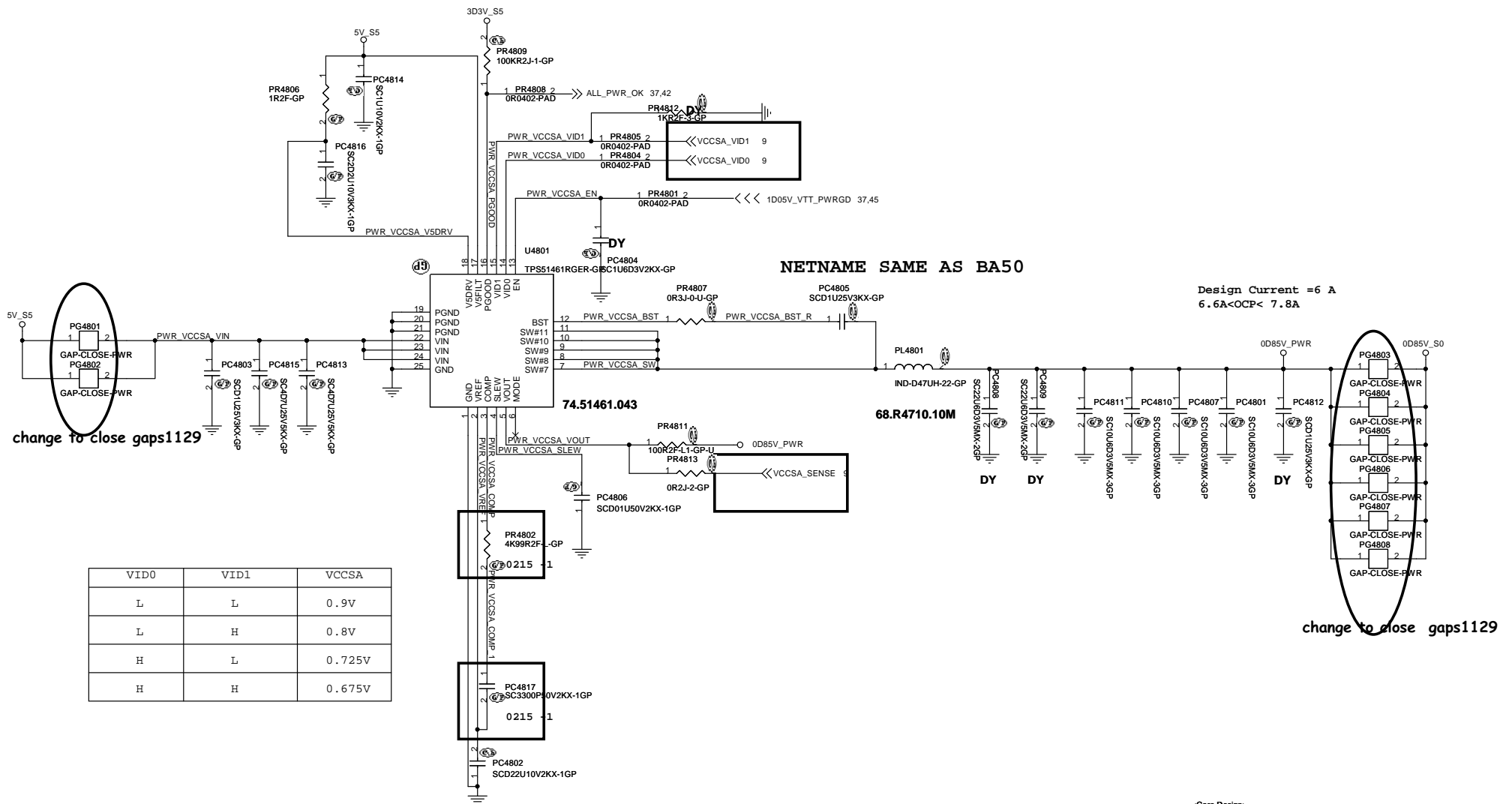
緯創資通 **Wistron Corporation**
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Taipai Hsien 221, Taiwan, R.O.C.

Title			
RT8207L			
Size Custom	Document Number		Rev
	BAD50-HC		-1
Dated	Thursday, March 29, 2012		Sheet 46 of 109

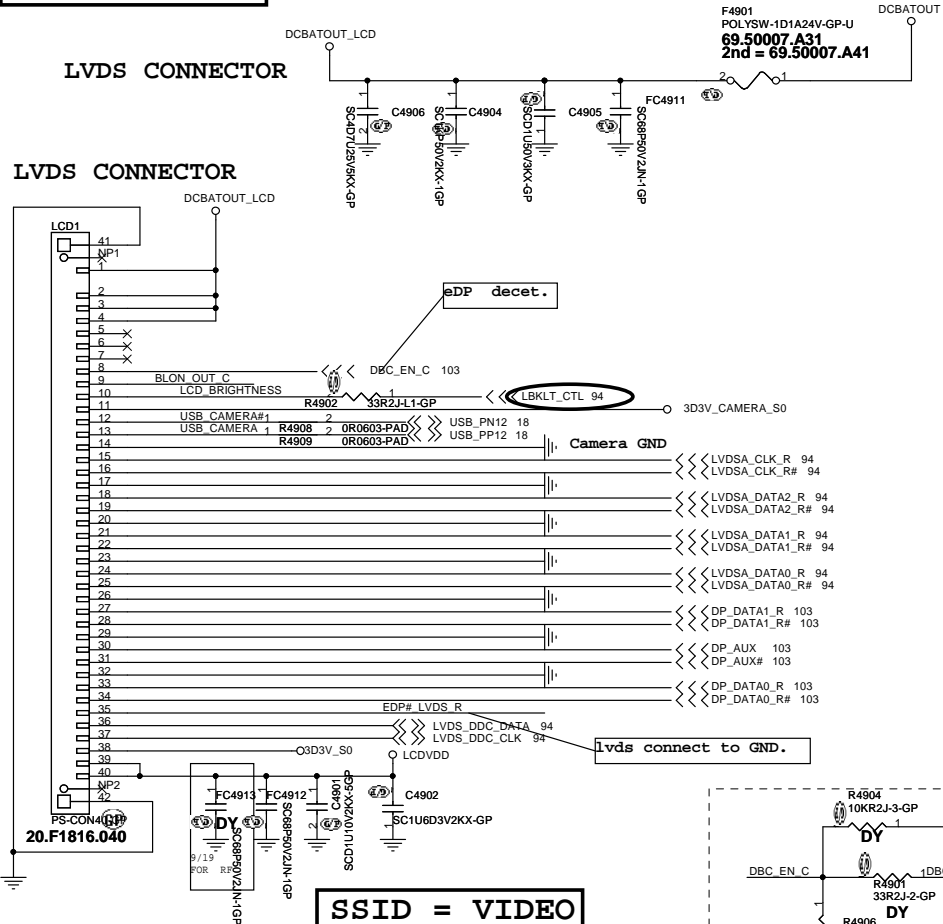
APW7153B for 1D8V_S0



TPS51461 for VCCSA

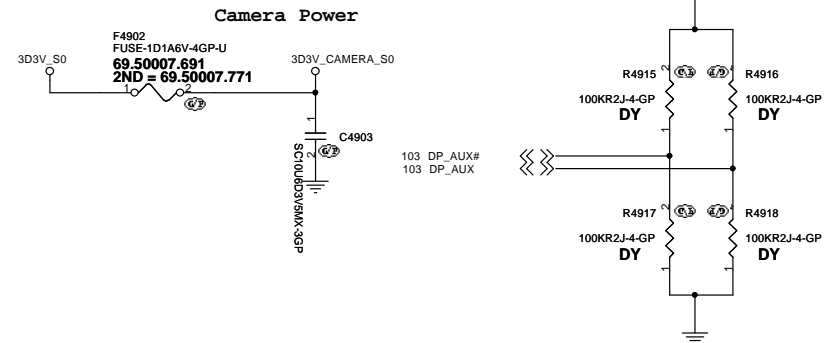
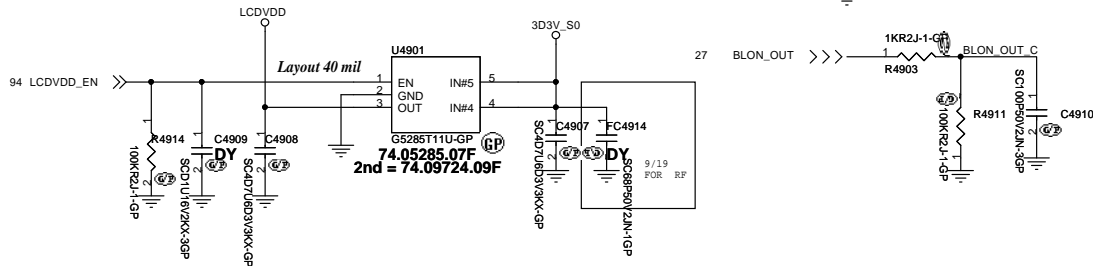


INVERTER POWER

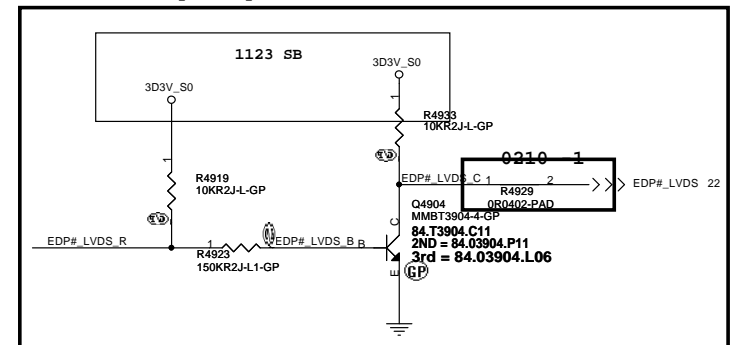


SSID = VIDEO

LCD POWER for ANNIE



Note: Place pull up resistor within 2 inch of CPU



LVDS0_CLK_R	D	1	FC9A01
LVDS0_CLK_R#	DY	1	ISCAD7P50V2CN-1GP 1 FC9A02
LVDS0_DATA2_R	DY	1	ISCAD7P50V2CN-1GP 1 FC9A03
LVDS0_DATA2_R#	DY	1	ISCAD7P50V2CN-1GP 1 FC9A04
LVDS0_DATA1_R	DY	1	ISCAD7P50V2CN-1GP 1 FC9A05
LVDS0_DATA1_R#	DY	1	ISCAD7P50V2CN-1GP 1 FC9A06
LVDS0_DATA0_R	DY	1	ISCAD7P50V2CN-1GP 1 FC9A07
LVDS0_DATA0_R#	DY	1	ISCAD7P50V2CN-1GP 1 FC9A08
LVDS_DDC_DATA	DY	1	ISCAD7P50V2CN-1GP 1 FC9A09
LVDS_DDC_CLK	DY	1	ISCAD7P50V2CN-1GP 1 FC9A10

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD Connector

Size

Document Number	
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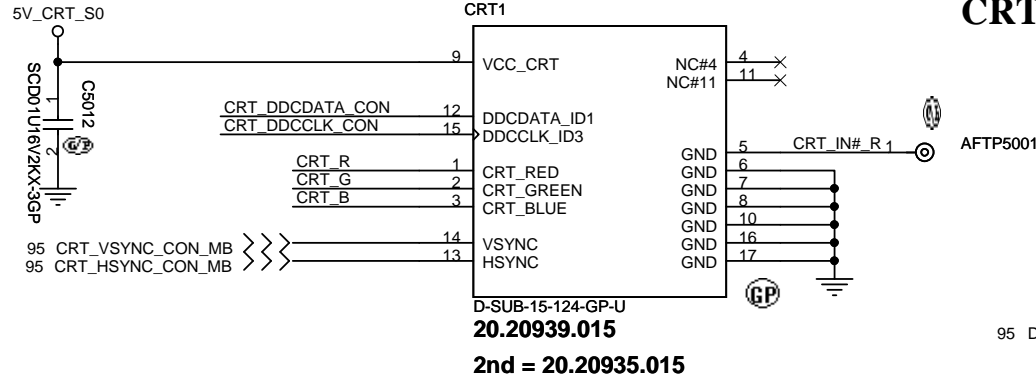
A3

BAD50-HC

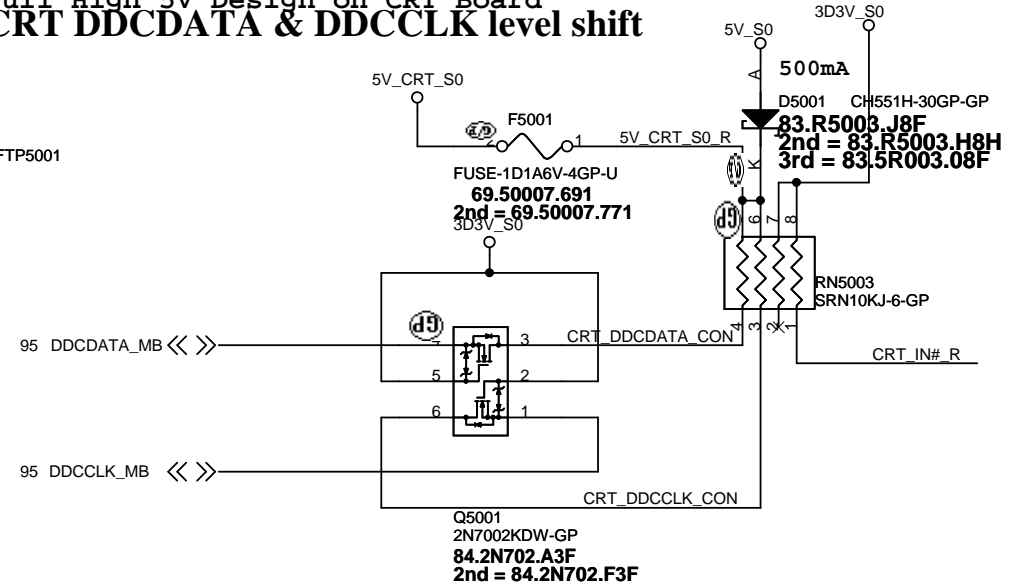
-1

Date: Thursday, March 29, 2012

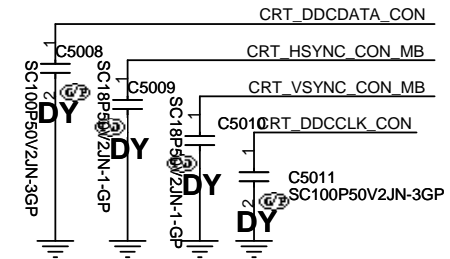
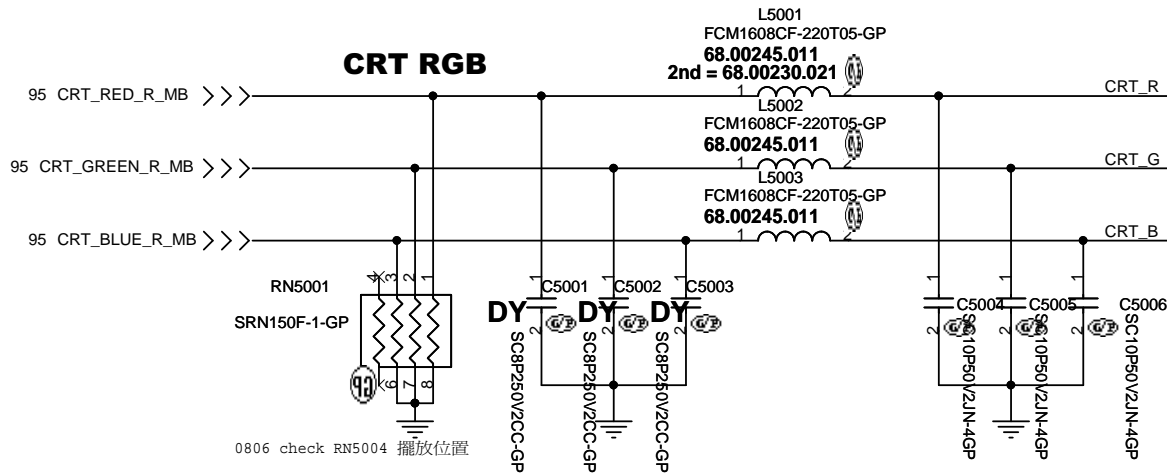
Sheet 49 of 109



Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift



CRT RGB



<Core Design>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size
A4

Document Number

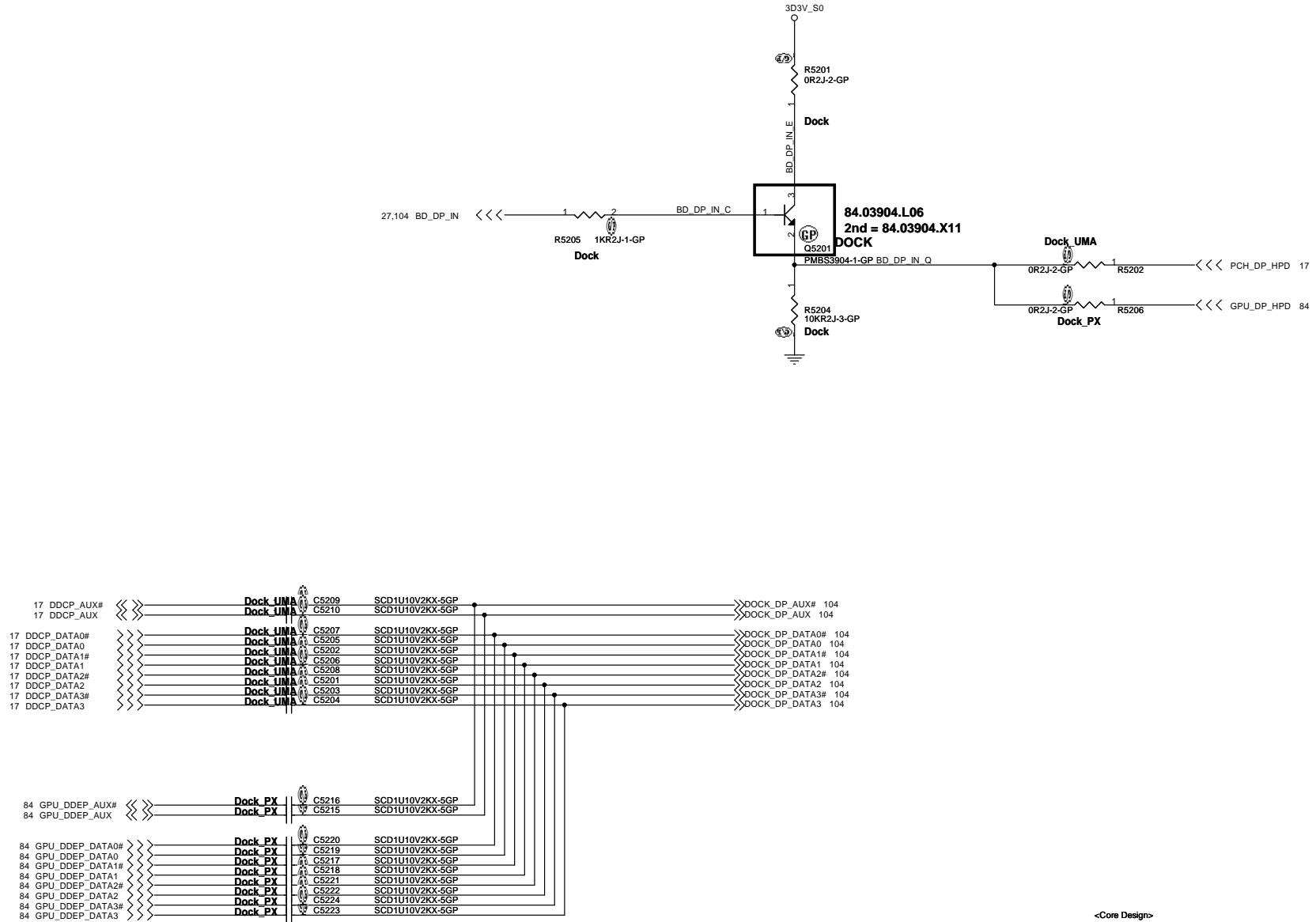
BAD50-HC

Rev
-1

Date: Saturday, March 03, 2012

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DP



(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
S-VIDEO		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 53 of 109

(Blanking)

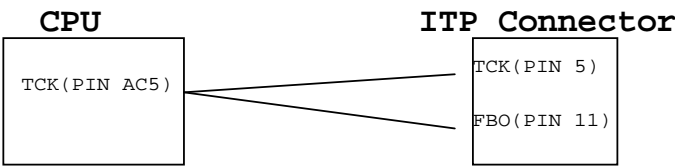
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 54 of 109

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

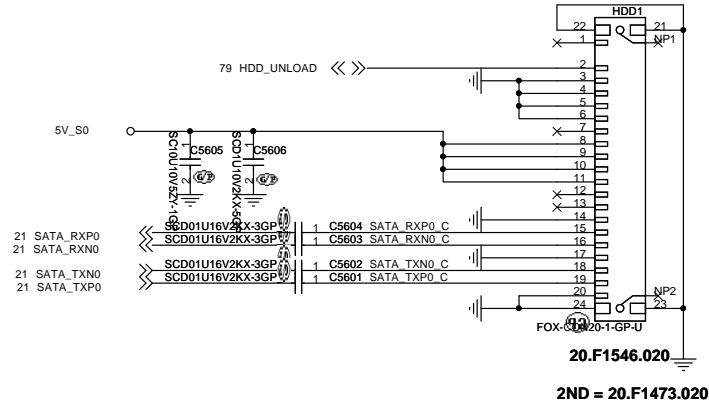


<Core Design>

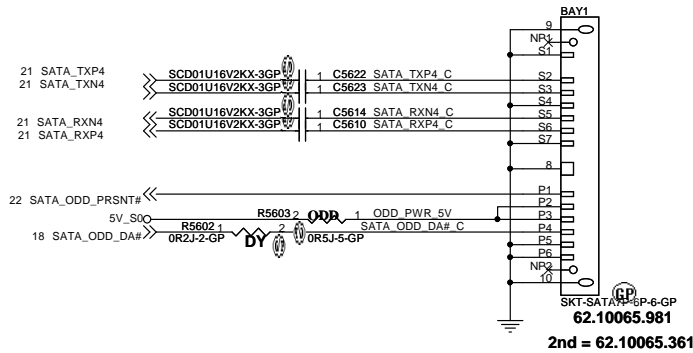
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP			
Size	Document Number		Rev
A4	BAD50-HC		-1
Date:	Friday, March 02, 2012	Sheet 55 of	109

SSID = SATA

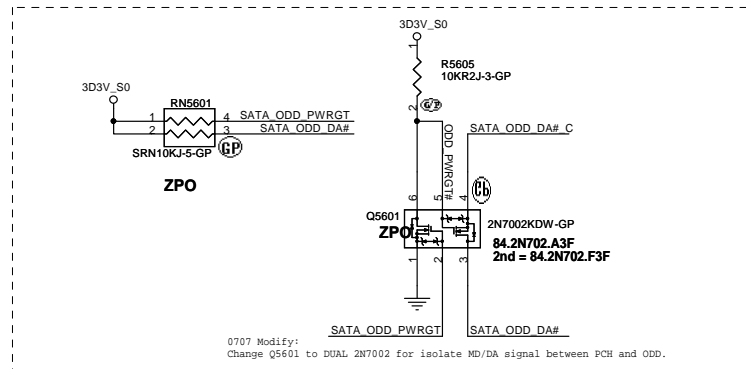
SATA HDD Connector



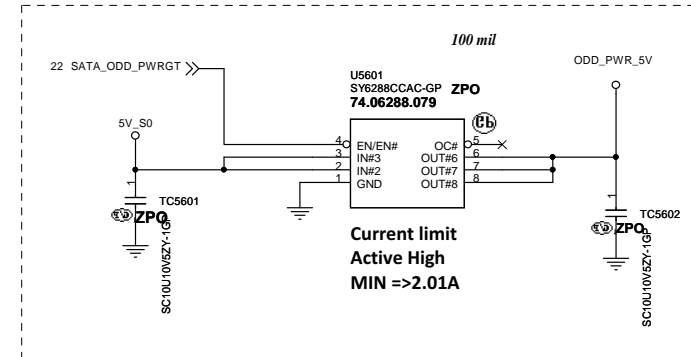
ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



SATA Zero Power ODD

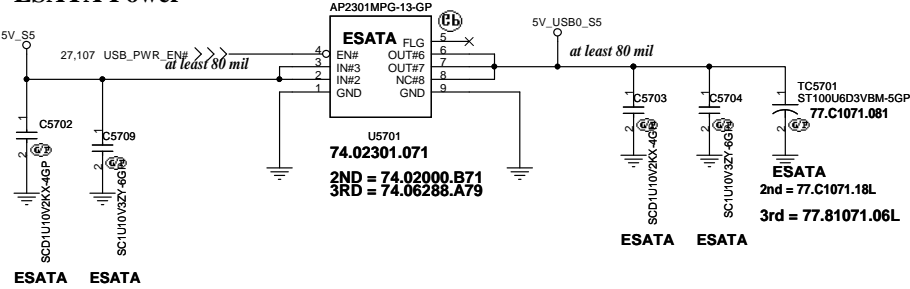


SATA Zero Power ODD



<Core Design>

ESATA Power

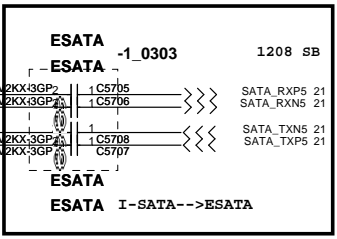
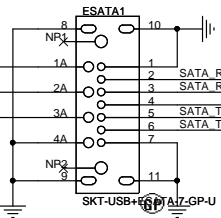


1208 SB

Bypass SATA redriver path
9/30

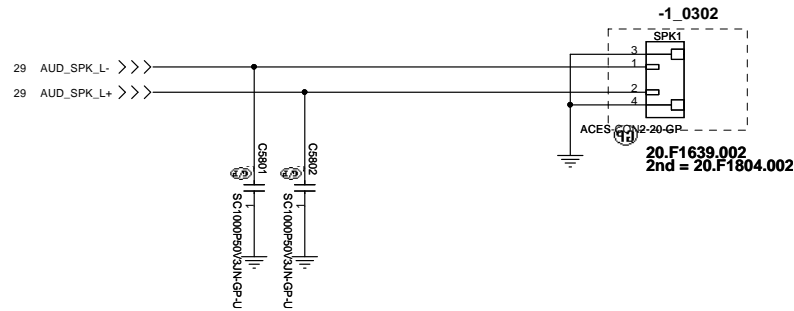
1208 SB

18 USB_PN9 >>>
18 USB_PP9 >>>
9/3

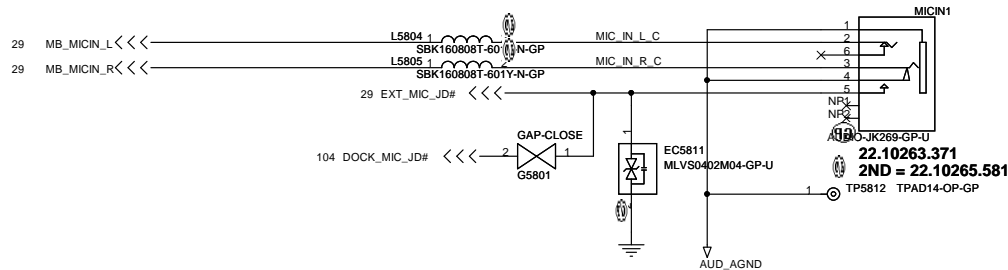


SSID = AUDIO

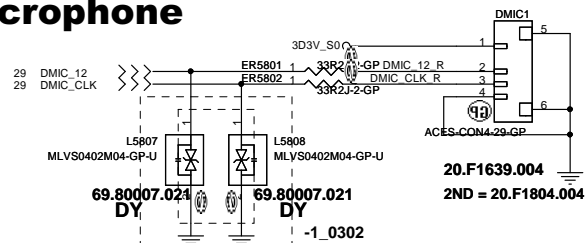
Speaker Connector



MIC IN

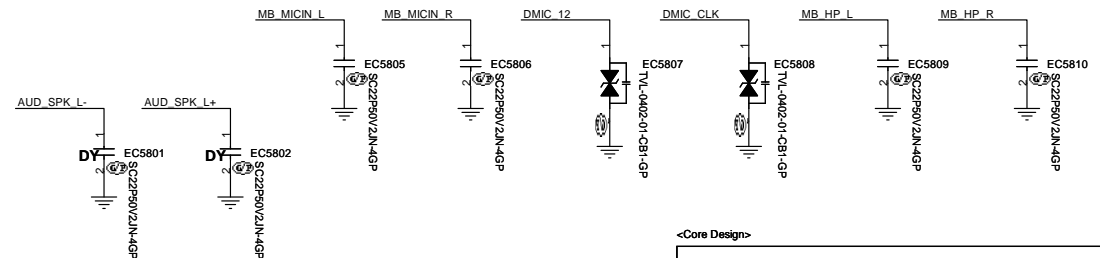
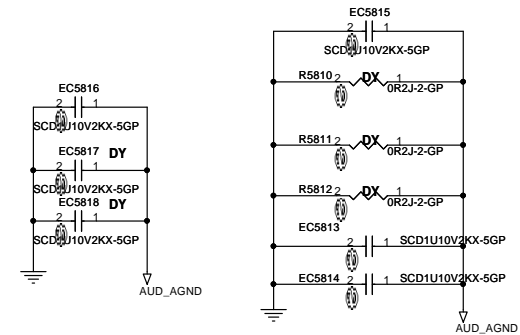
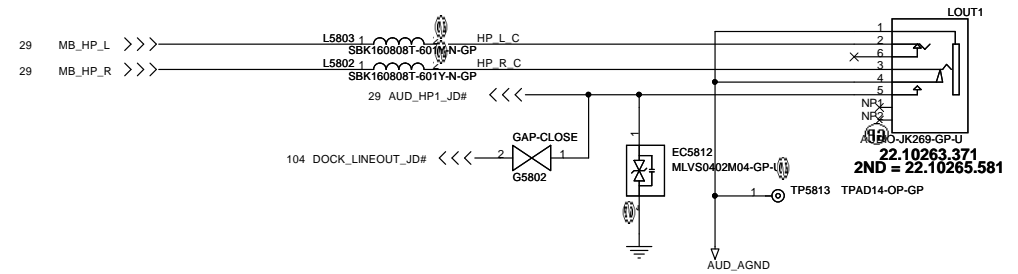


Internal Microphone



(Varistor)
Need confirm with EMI :
69.80007.021 or 69.80024.011 ?

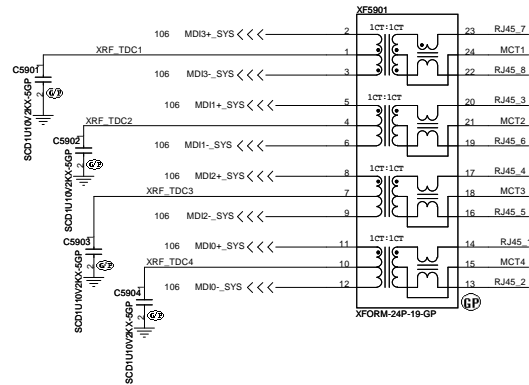
LINE OUT



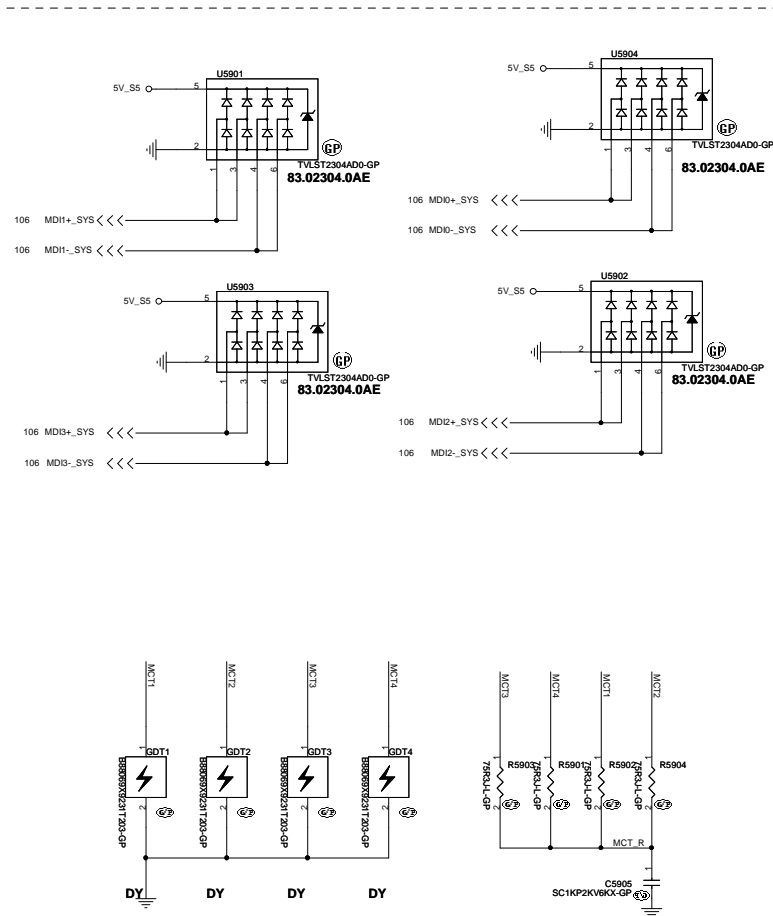
GIGA Lan Transformer

SSID = LOM

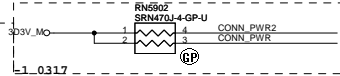
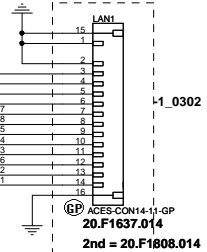
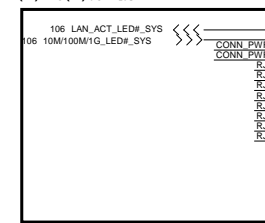
LAN MDI Off-Page



For EMI



LED COLOR
10(+): 9(-)::GREEN
12(+): 13(-)::ORANGE



1209 SE

[illegible]

The schematic diagram illustrates the SPI interface for the MX25L6406E2-125-GP dual ROM. The ROM is connected to a microcontroller (U6003) via SPI signals: CS#, SO/SDI, SCLK, and SI/SSDO. The ROM is also connected to a 3D3V_S5 power supply through a 100nF capacitor. The microcontroller is connected to a 3D3V_S5 power supply through a 100nF capacitor. The ROM is labeled 'DUAL ROM' and '72.25640.D01'.

PCH and EC length less than 6.5 inch

Control

[illegible]

for ENE FAE suggest, SPICS# is push-pull pin,
don't need to pull high

[illegible]

The diagram illustrates the SPI interface circuit. It consists of three signal lines: SPICLK_1, SPI_DO, and SPIDI. Each line is connected to a pull-up resistor (EC6004, EC6005, and EC6006 respectively) and a diode (DY) to ground.

«Core Design»

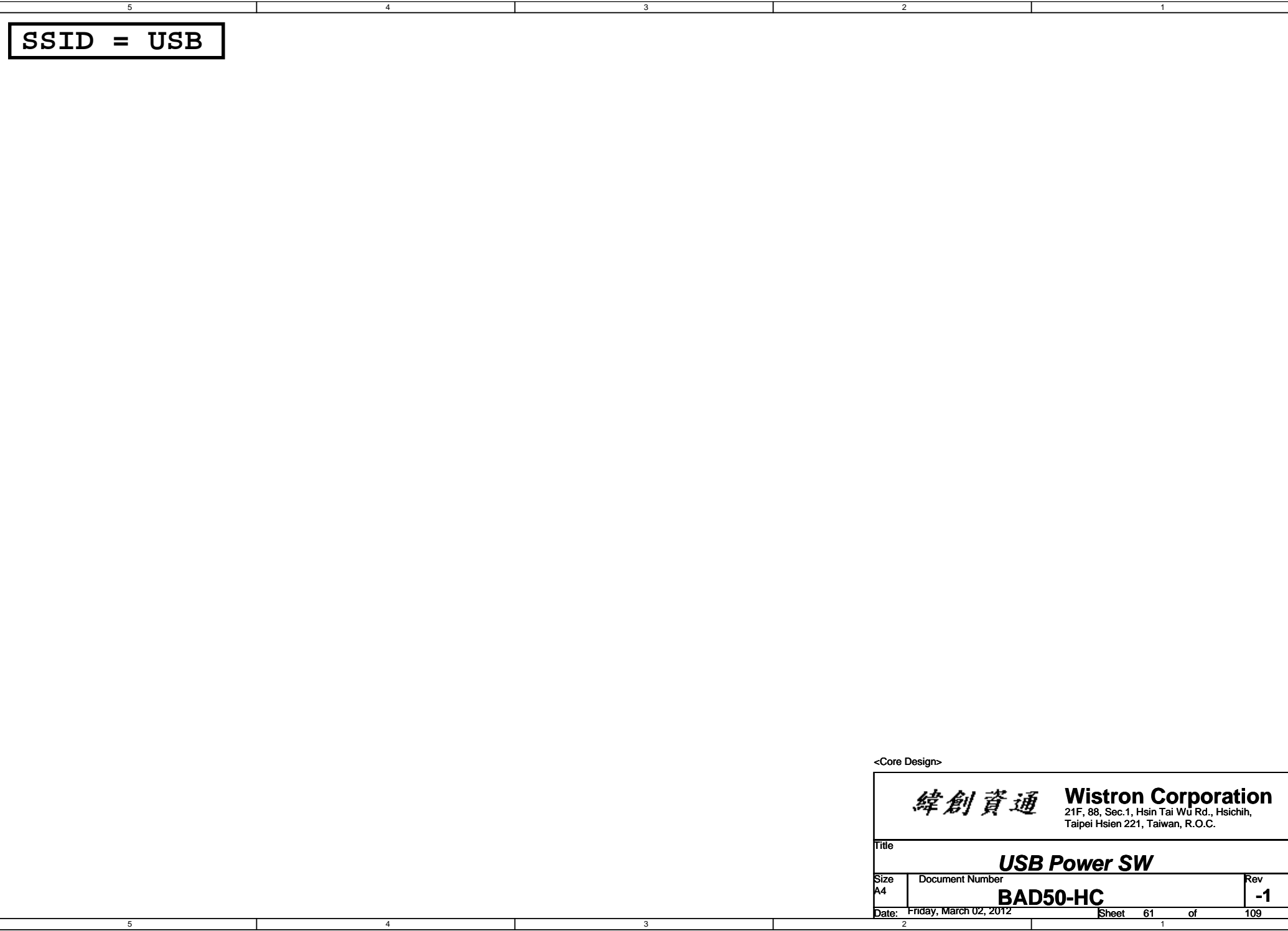
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC
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Size	Document Number
Custom	BAD50-HC

Rev
1

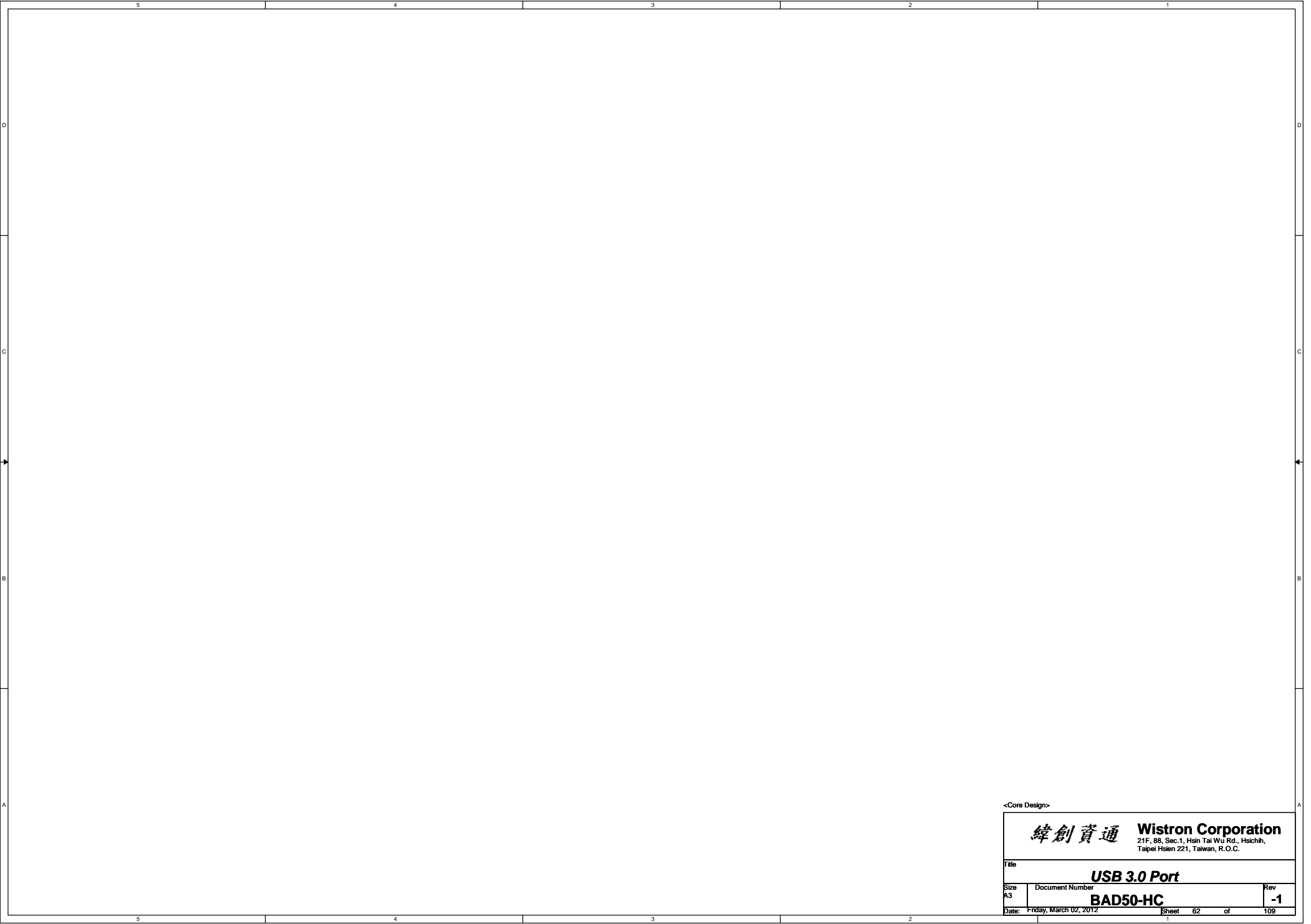
Date: Thursday, March 29, 2012	Sheet 60 of 109
--------------------------------	-----------------



SSID = USB

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
USB Power SW		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 61 of 109



<Core Design>

Title		Size		Date:	
USB 3.0 Port		A3		Friday, March 02, 2012	
Document Number		Rev		Sheet	
BAD50-HC		-1		62 of 109	

SSID = User.Interface
Bluetooth Module conn.

1220 SB del

EC6302 put near BLUE1 / all USB put one
choke near connector by EMI request

ANNIE Bluetooth Module

<Core Design>

緯創資通		Wistron Corporation	
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Title			
Bluetooth			
Size	Document Number		Rev
A4	BAD50-HC		-1
Date:	Friday, March 02, 2012		Sheet 63 of 109

JE40 delete FP function



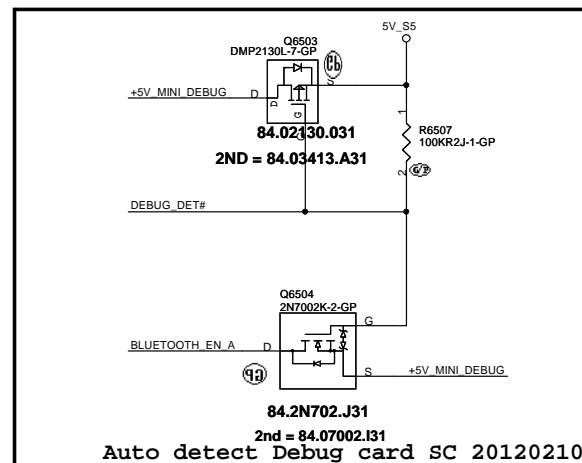
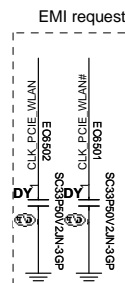
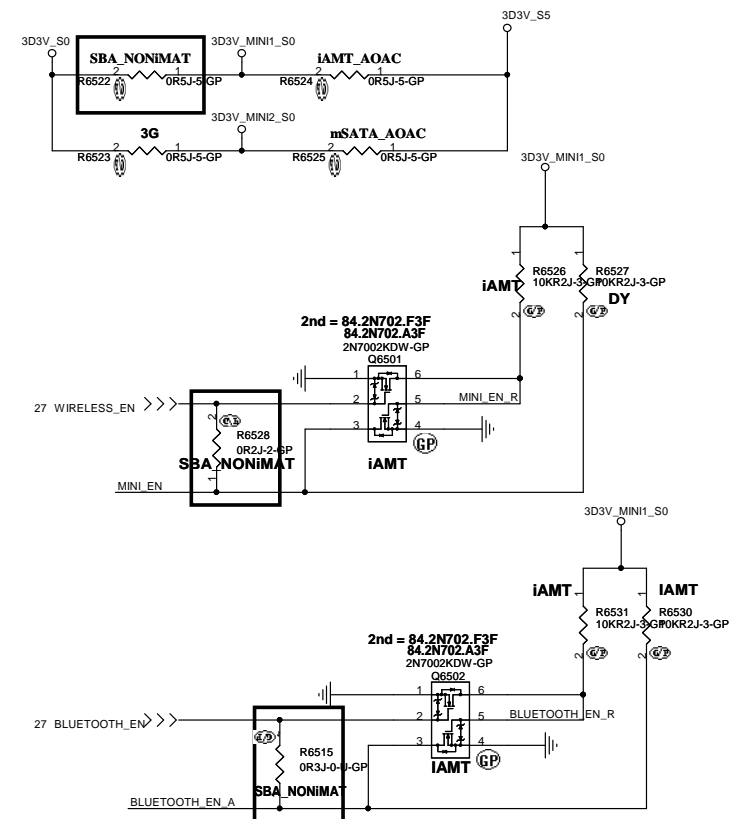
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

RESERVED

Rev	-1
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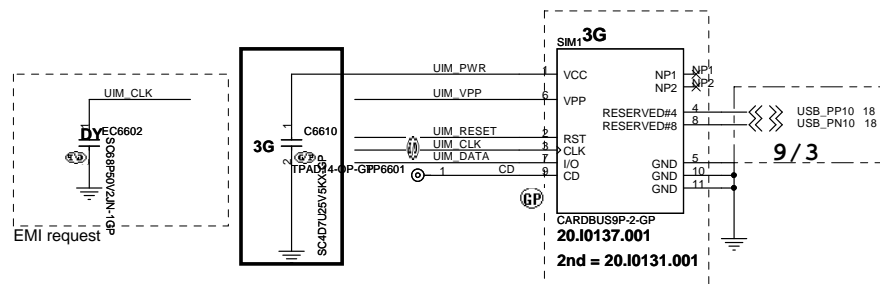
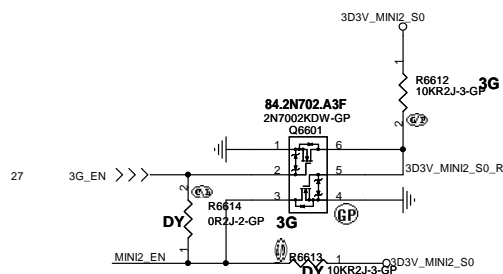
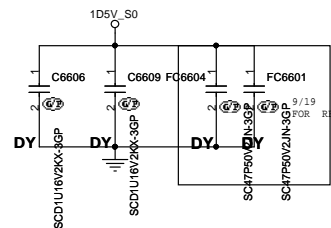
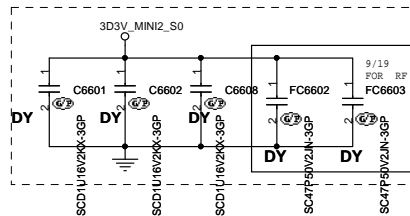
Mini Card Connector(802.11a/b/g/n)



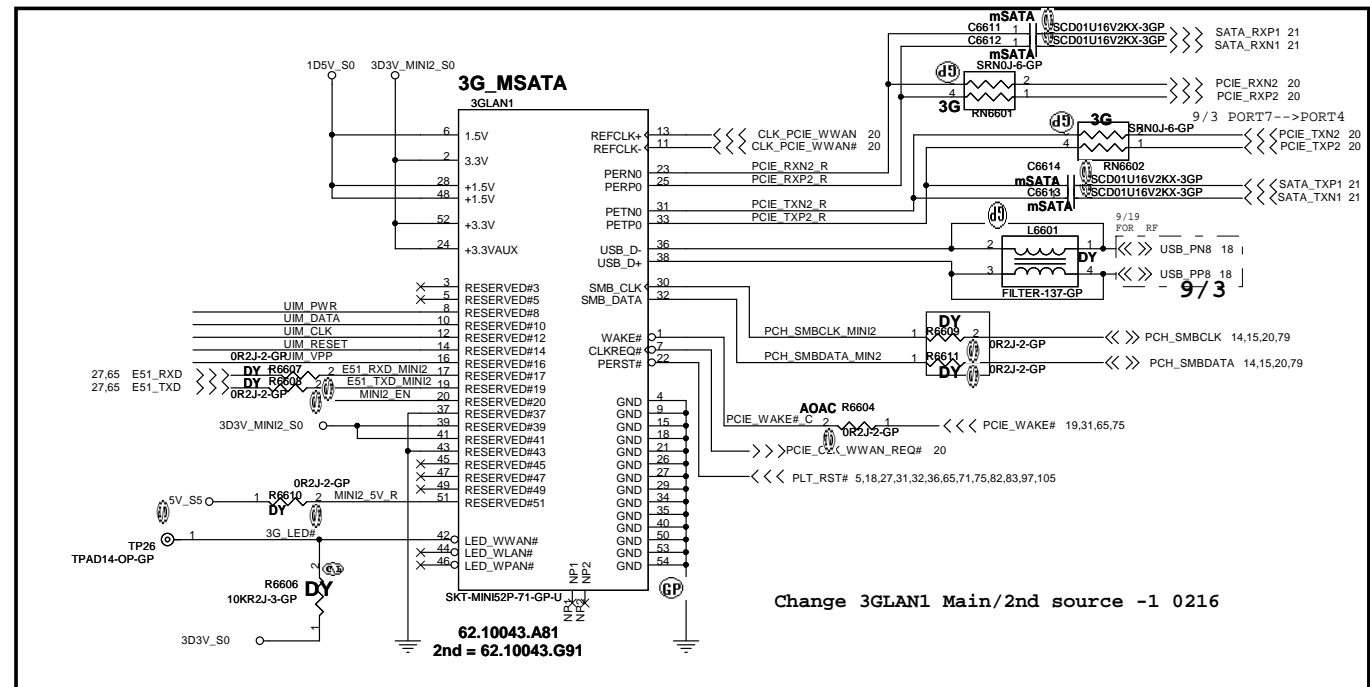
```
SSID = Wireless
```

20100712 V1.5

Place near MINI Card CONN



Mini Card Connector(WWAN)



Change 3GLAN1 Main/2nd source -1 0216

-1_0304

<Core Design>

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Title	
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WWAN Connector		
Size	Document Number	Rev

Size A3	Document Number BAD50-HC	Rev -1
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Date: Monday, April 02, 2012 Sheet 66 of 109

(Blanking)

<Core Design>

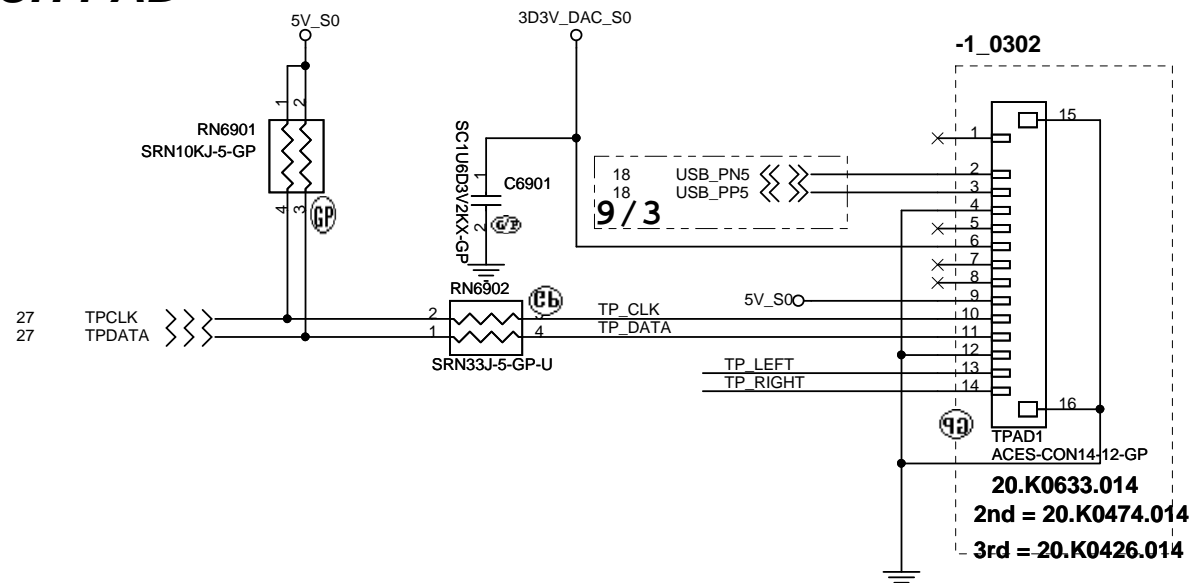
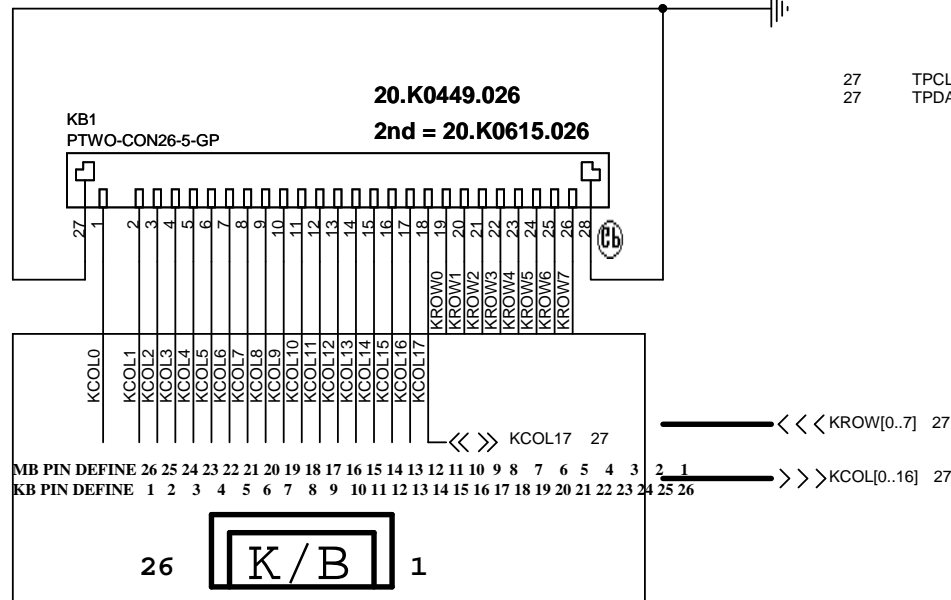
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
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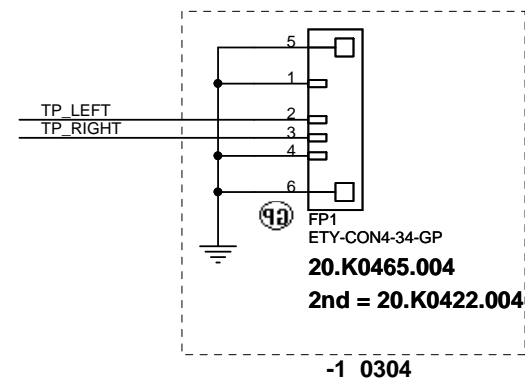
SSID = KBC

TOUCH PAD

Internal KeyBoard Connector



Rubber Dome



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size
A4

Document Number

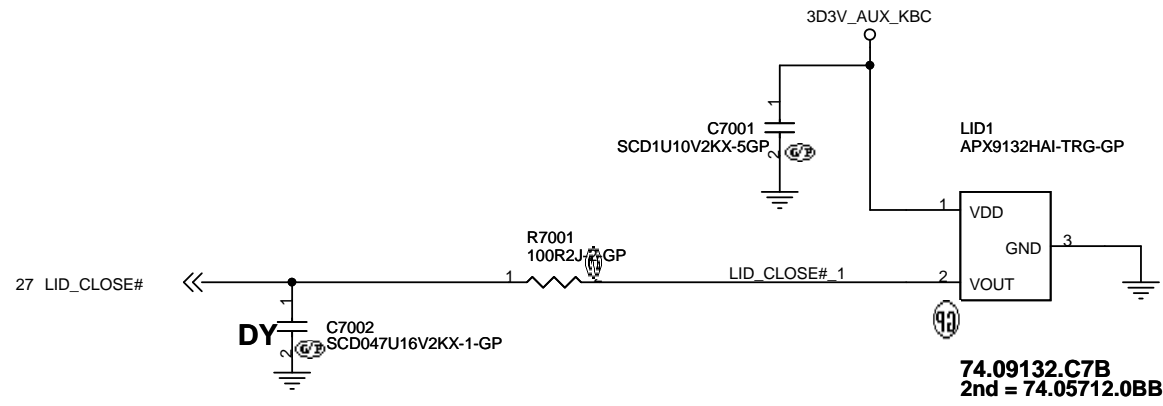
BAD50-HC

Rev

-1

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

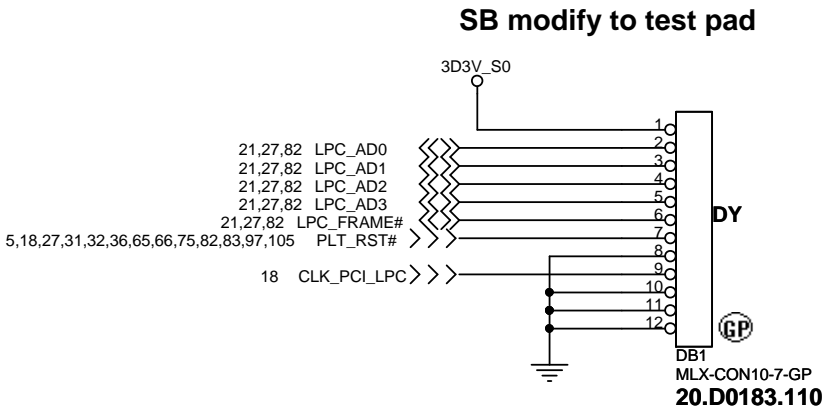
Document Number

BAD50-HC

Rev
-1

Date: Saturday, March 03, 2012

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size A4	Document Number BAD50-HC		Rev -1
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(Blanking)

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number BAD50-HC		Rev -1
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<Core Design>

緯創資通			Wistron Corporation		
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Title					
Reserved					
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SSID = SDIO

SD/XD/MS Card Reader

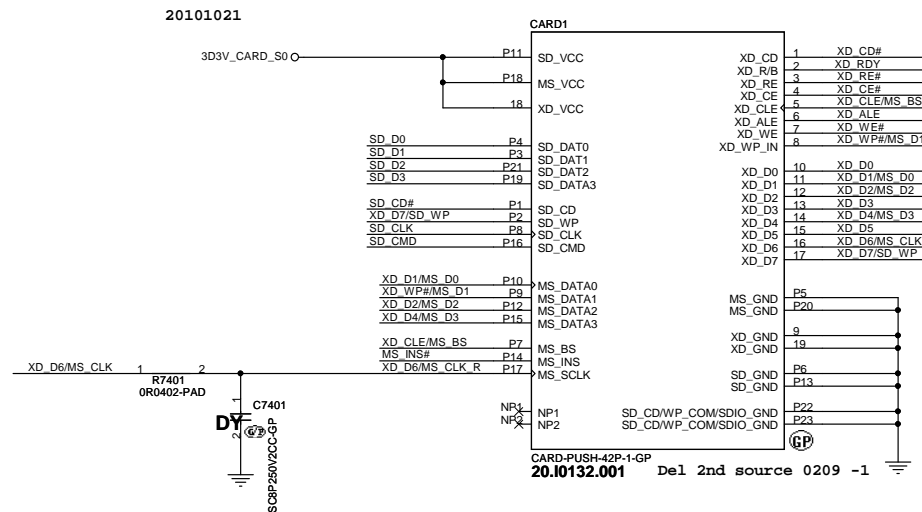
32 XD_CD# <<>> _____
32 SD_D1 <<>> _____
32 SD_D0 <<>> _____
32 SD_D2 <<>> _____
32 SD_D3 <<>> _____

32 SD_CLK <<>> _____
32 SD_CMD <<>> _____

32 SD_CD# <<>> _____
32 MS_INS# <<>> _____

32 XD_RDY <<>> _____ SP1(N0 SD_D7)
32 XD_RE# <<>> _____ SP2(N0 SD_D6)
32 XD_CE# <<>> _____ SP3(N0 SD_D5)
32 XD_WE# <<>> _____ SP4(N0 SD_D4)
32 XD_CLE/MS_BS <<>> _____ SP5
32 XD_ALE <<>> _____ SP6
32 XD_WP#/MS_D1 <<>> _____ SP7
32 XD_D0 <<>> _____ SP8(N0 MS_D4)
32 XD_D1/MS_D0 <<>> _____ SP9
32 XD_D2/MS_D2 <<>> _____ SP10

32 XD_D3 <<>> _____ SP11(MS_D6)
32 XD_D4/MS_D3 <<>> _____ SP12
32 XD_D5 <<>> _____ SP13
32 XD_D6/MS_CLK <<>> _____ SP14
32 XD_D7/SD_WP <<>> _____ SP15



<Core Design>

緯創資通

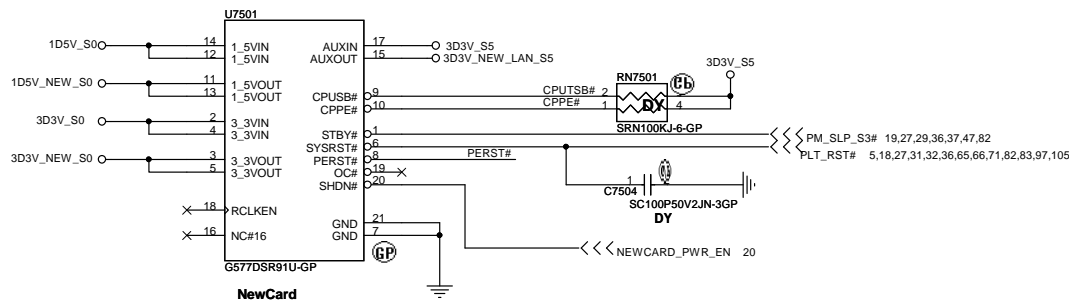
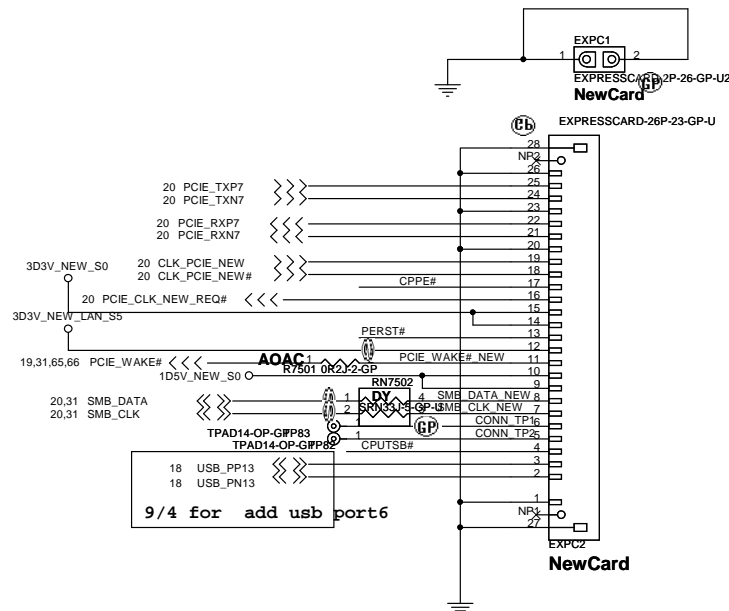
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CARD Reader CONN
Size	Document Number	Rev	-1
A3	BAD50-HC		
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SSID = ExpressCard

For Expresscard socket

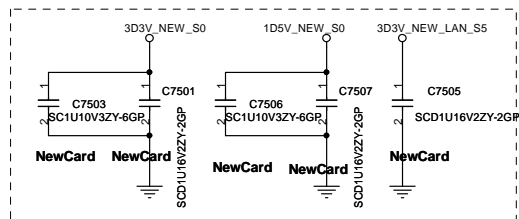
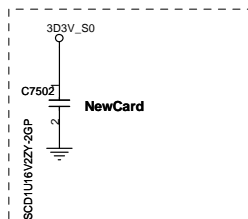
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



Place them Near to Chip

Place them Near to Connector

For EMI

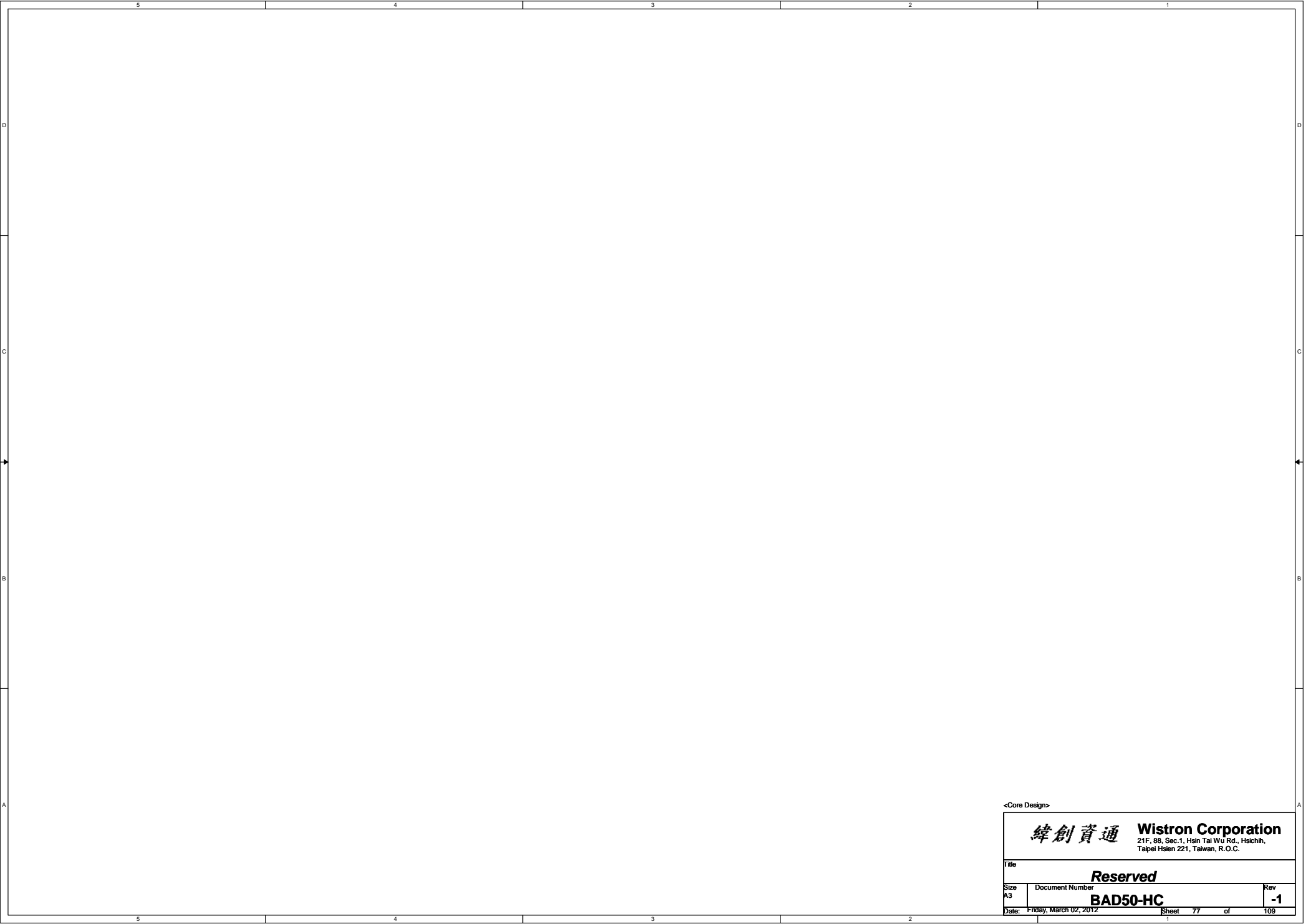


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			New Card	
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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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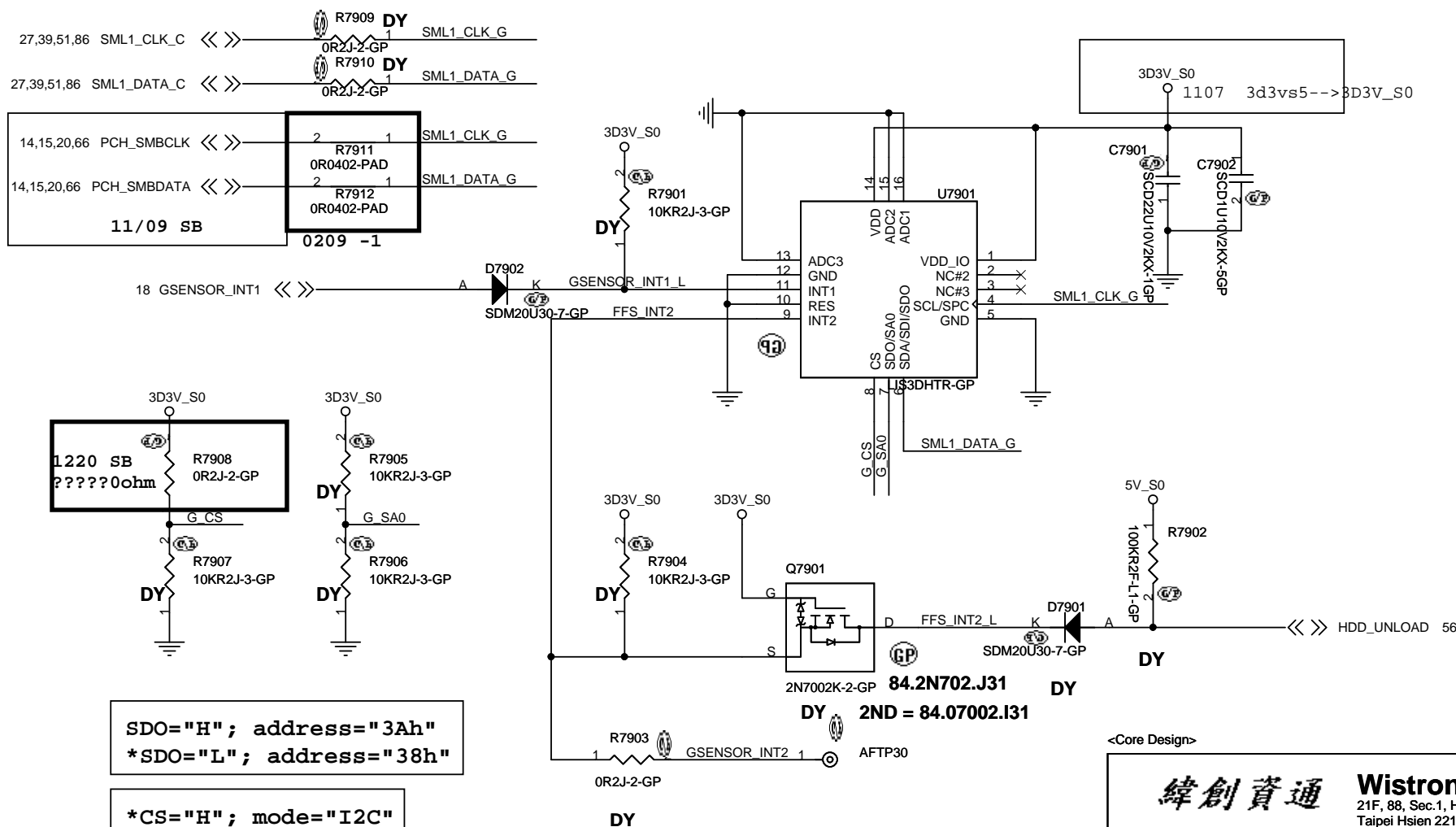
(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
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Free Fall Sensor

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



```
*CS="H"; mode="I2C"
CS="L"; mode="SPI"
```

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Free Fall Sensor

BAD50-HC

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(Blanking)

<Core Design>

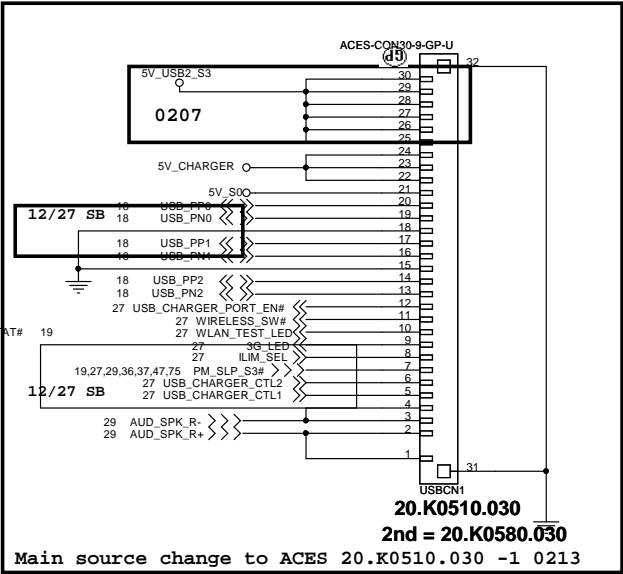
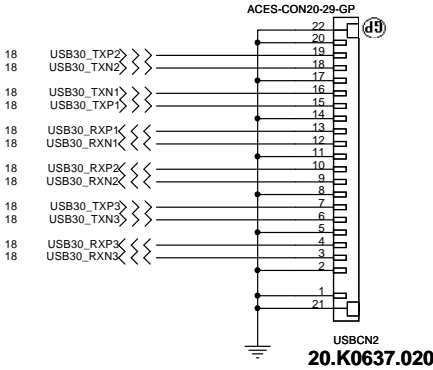
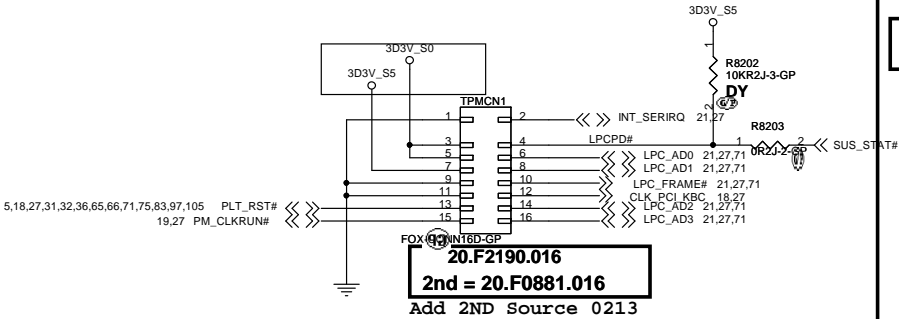
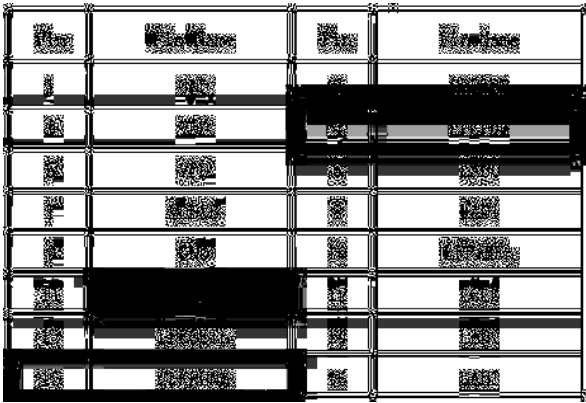
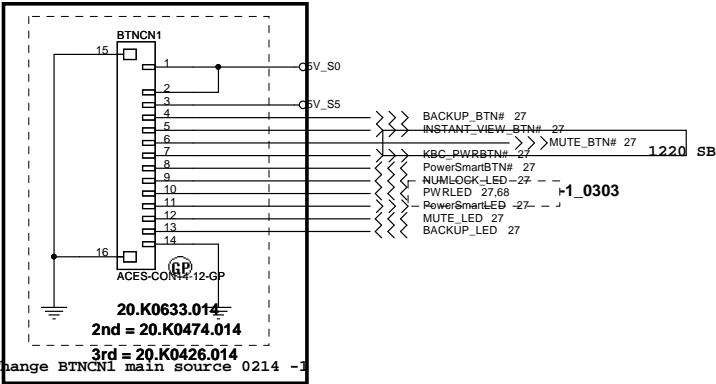
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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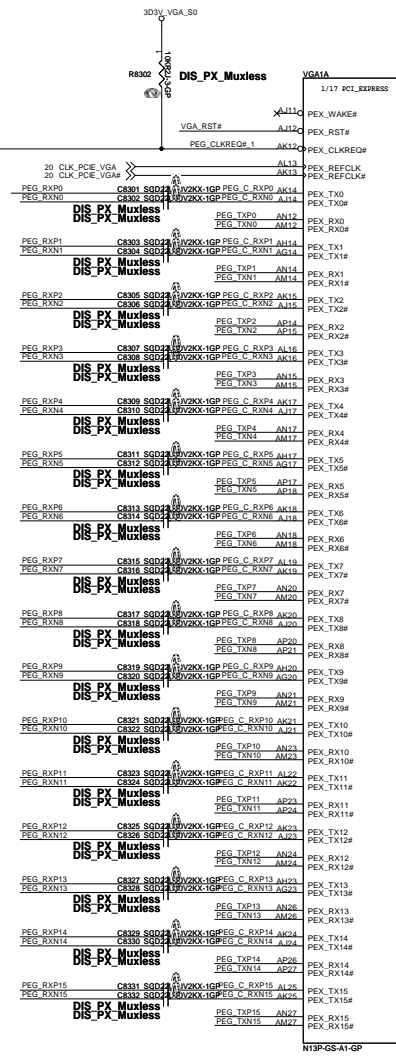
(Blanking)

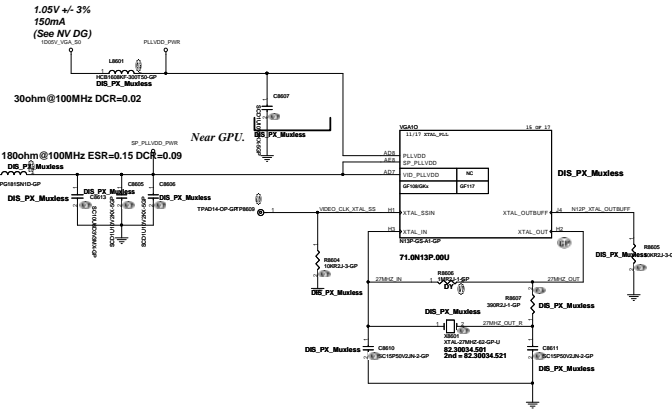
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
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PWRCN1 FFC 異面







4.99 k	9000	0000
50.0 k	9001	0001
15.0 k	9008	0010
20.0 k	9011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
40.3 k	1111	0111

Table 109. Display Link to SDRx_EXPOSED Bit Mapping

Deal 1 Job Node	SP4/B	SC02 EXPOSED = 0	SC02 EXPOSED = 0
EP0	SC01 EXPOSED = 1		SC01 EXPOSED = 0
EP1	SC02 EXPOSED = 1	SC02 EXPOSED = 0	SC02 EXPOSED = 0
EP2/B	SC03 EXPOSED = 1		SC03 EXPOSED = 0
Split Node	SP4/B		
	EP0	SC01 EXPOSED = 1	SC01 EXPOSED = 0
	EP1	SC02 EXPOSED = 1	SC02 EXPOSED = 0
	EP2	SC03 EXPOSED = 1	SC03 EXPOSED = 0
	EP3	SC04 EXPOSED = 1	SC04 EXPOSED = 0

Table 106. 3GIO_PADCFG Strap Setting

0000-0101	RESERVED	
0110	Notobank	Notobank: Default
0111-1111	RESERVED	

	ROM_SI	ROM_SO	ROM_CLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P_GS ES	PH 10K ohm	PH 4.99K ohm	PH 45K, 3ohm	PL 34.8K ohm	PH 20K ohm	PH 15K ohm	PH 20K ohm	PH 20K ohm
N13P_GL	PH 10K ohm	PL 15K ohm	PH 45K, 3ohm	PL 34.8K ohm	PH 10K ohm	PH 15K ohm	PH 20K ohm	PH 20K ohm

STRAP0	USER[0]=1		STRAP1	3GIO_PADCFG[0]=0	
	USER[1]=1	USE 111 (45K)		3GIO_PADCFG[1]=1	USE 0110 (35K)
	USER[2]=1			3GIO_PADCFG[2]=1	
	USER[3]=1			3GIO_PADCFG[3]=0	

Table 105. User Straps

00000	BCA	1024 x 768	-/-	
00001	BCA	1024 x 768	+/-	
00010	WGA	1280 x 1024	-/-	
00011	WGA+	1400 x 1050	-/-	
00100	EBGA	1600 x 1200	+/-	
00101	EBGA	2048 x 1536	+/-	
00110	WGA+	1400 x 1050	-/-	
00111	WGA	800 x 600	-/-	
00000 - 00000				Customer default [Default]
00000				00000 is default

	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

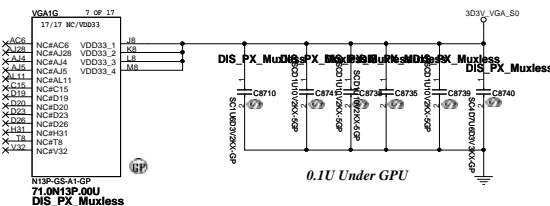
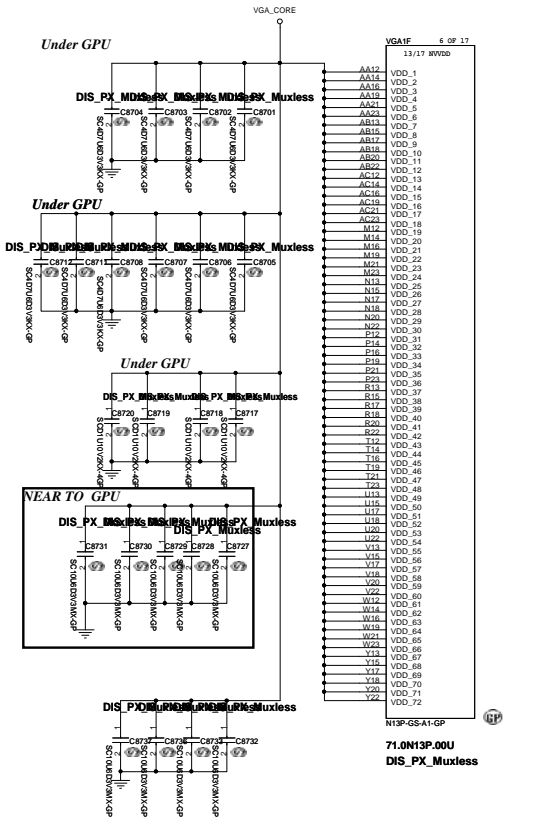
	N13P-GS DEV ID: 0x0FD2	N13P-GS-ES DEV ID: 0x0FDB	N13P-GL DEV ID: 0x0DE9		
STRAP2	15Kohm 64.15026.6DL	20Kohm 64.20025.6DL	10Kohm 63.10334.1DL		

	DEVID	ROM CLK	MDR2
NIM-02-A1	HUNT2	T000	BLSA SWT
		D010	SELVDC

[illegible]

OrderID	Logical shipping number SH01	Logical shipping number SH02	Logical shipping number SH03	Logical shipping number SH05	
Group 10000000000000000000					
	1	0	0	0	202-0000
	0	1	1	0	Group 20 20, 30, 40
	0	0	0	1	Group 10 10, 100
	1	0	0	1	202-0000
	1	1	1	1	202-0000
	0	1	1	0	202-0000
	1	0	1	1	202-0000
	1	0	0	0	202-0000
	1	0	0	1	202-0000

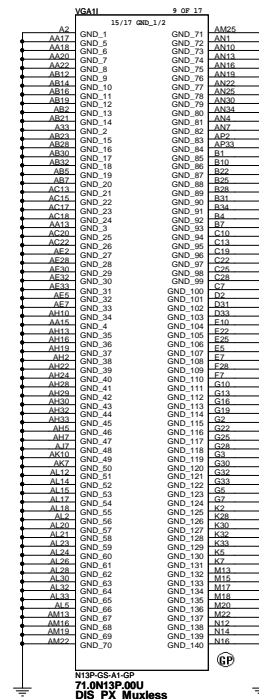
EDP 50A (TDP 37W)



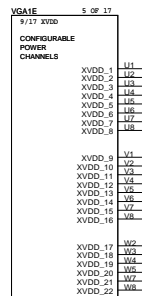
0.1U Under GPU

4.7U NEAR TO GPU

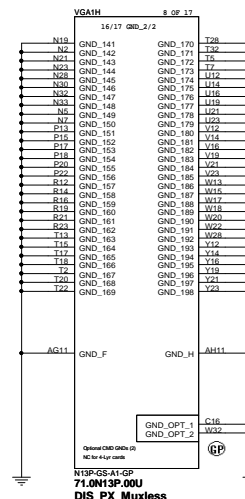
1U NEAR TO GPU



71.0N13P.00U
DIS_PX_MUXless

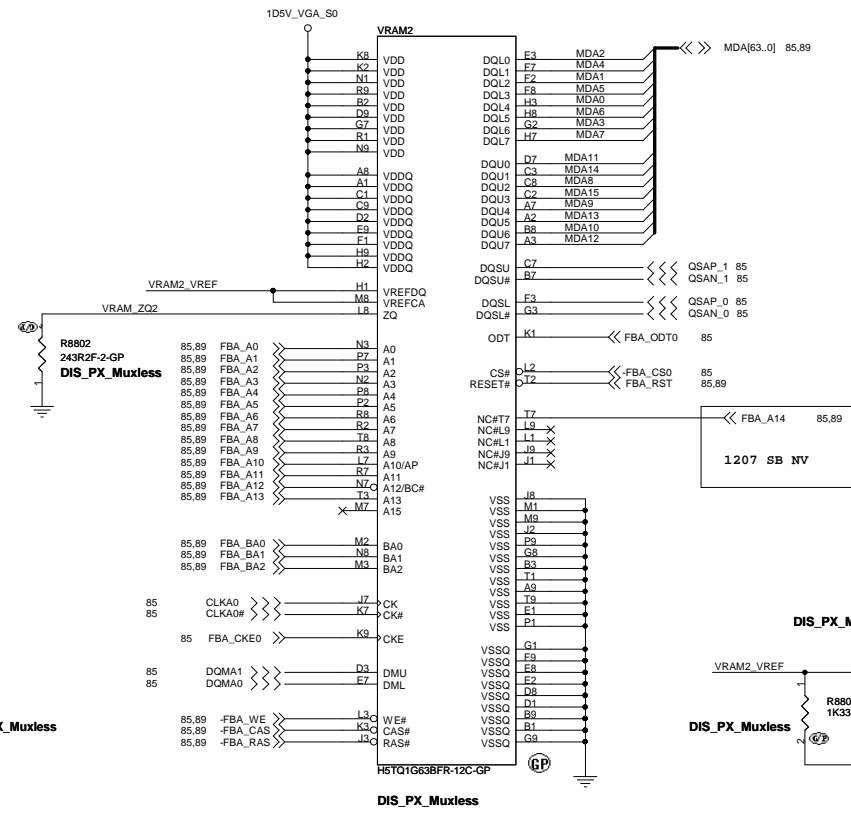


71.0N13P.00U
DIS_PX_MUXless



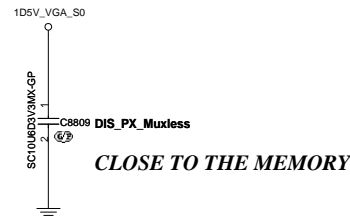
71.0N13P.00U
DIS_PX_MUXless

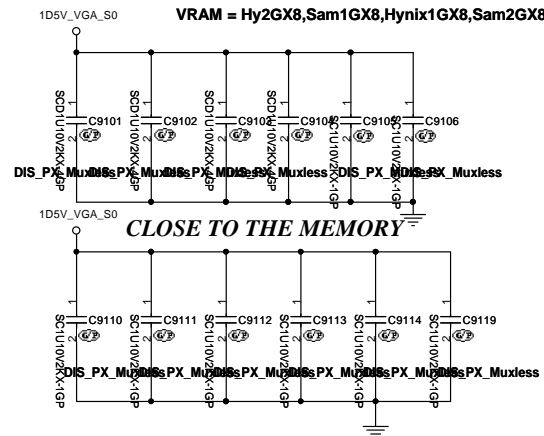
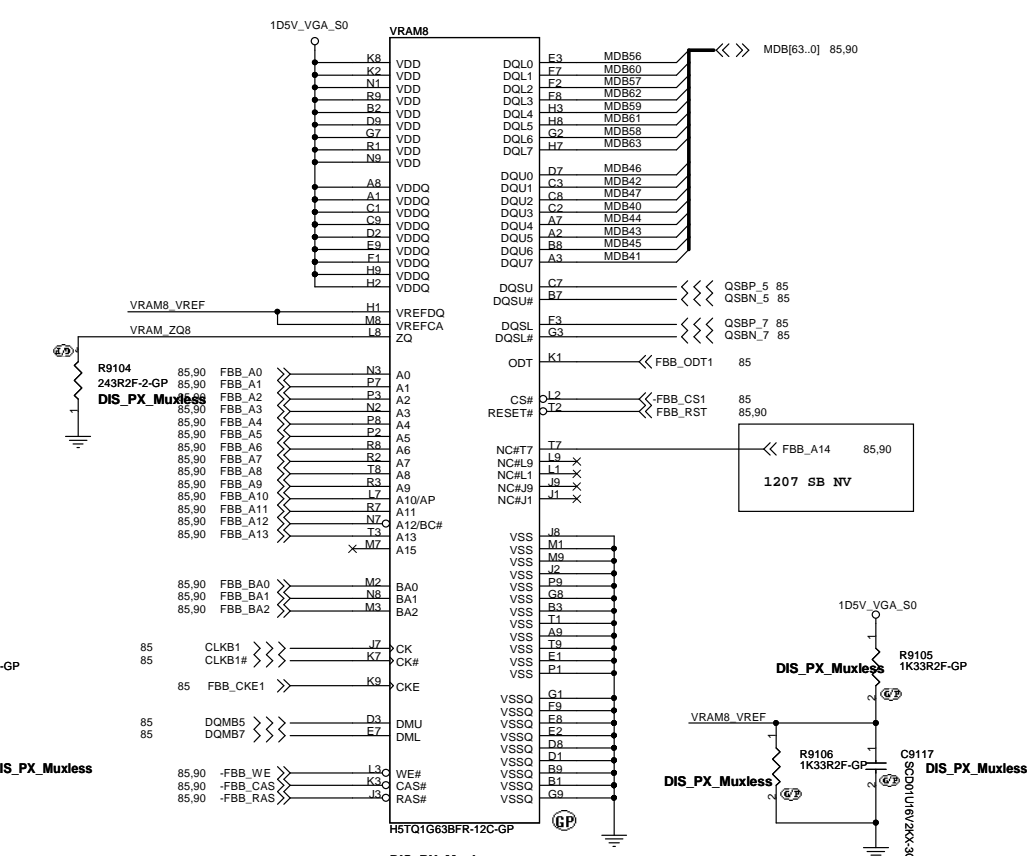
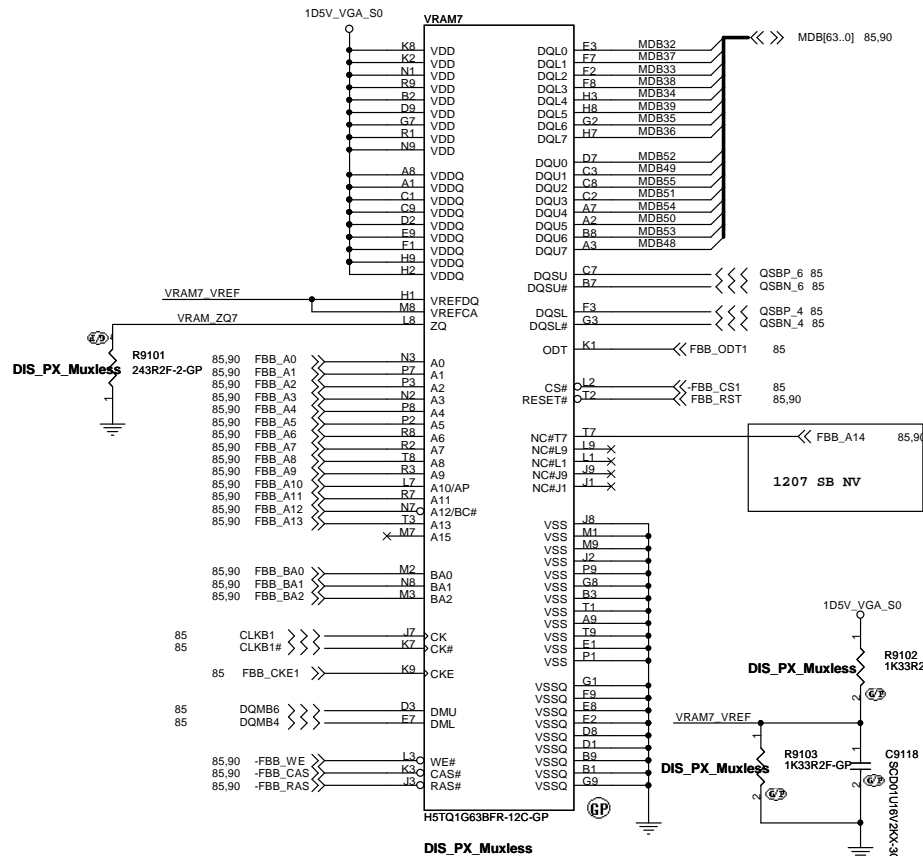
Core Design



VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8
FB CMD mapping Mode D-N12x

**DG requires 4x0.1uF and 8x1.0uF per
VRAM chip**





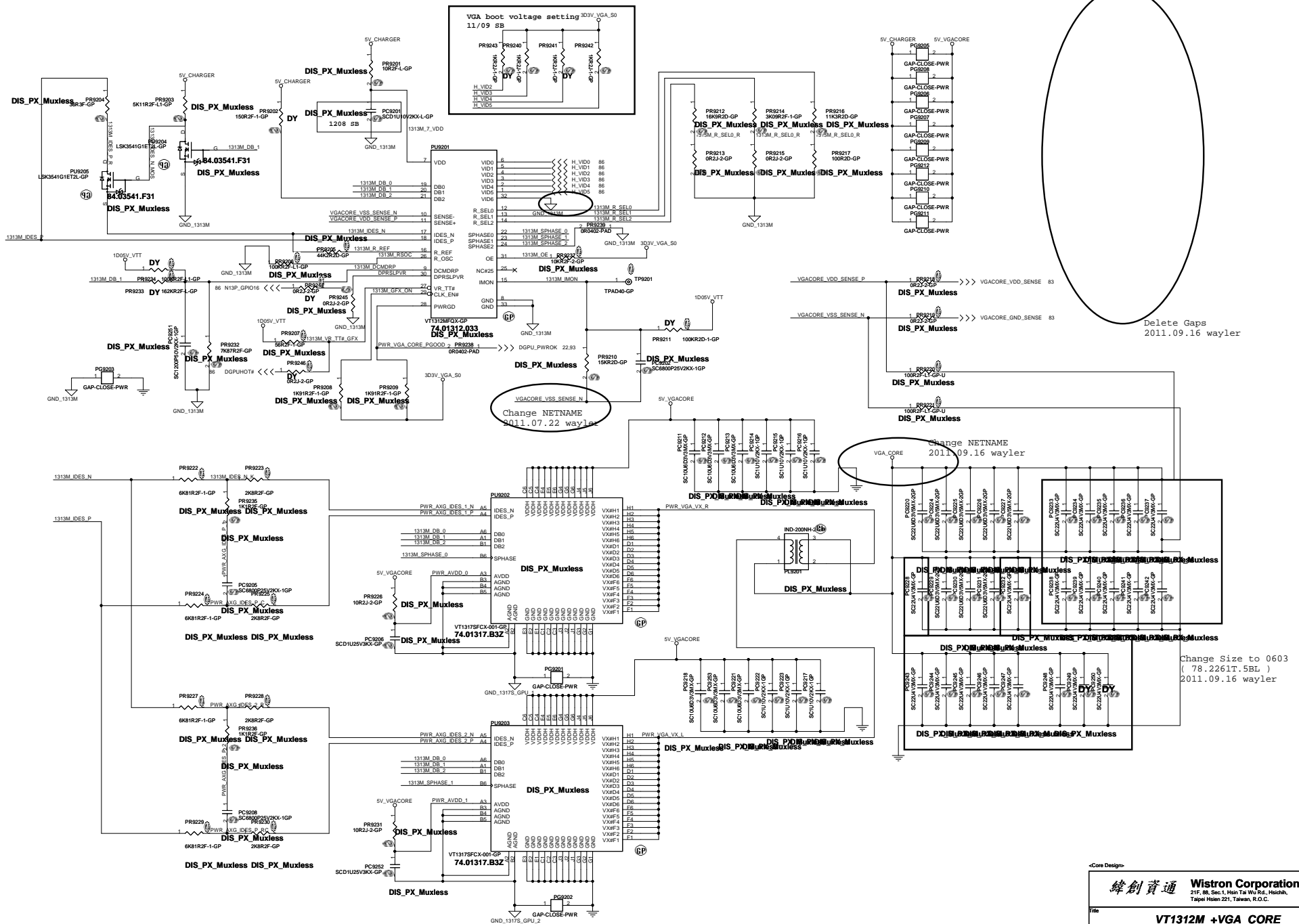
CLOSE TO THE MEMORY

VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

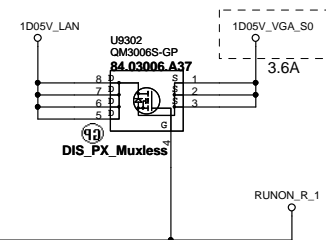
VRAM SAMSUNG 1Gb VR.1GB0B.006

VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005

VRAM HYNIX 2Gb VR.2GB0G.001



1.05V to 1.05V_VGA_S0 Transfer

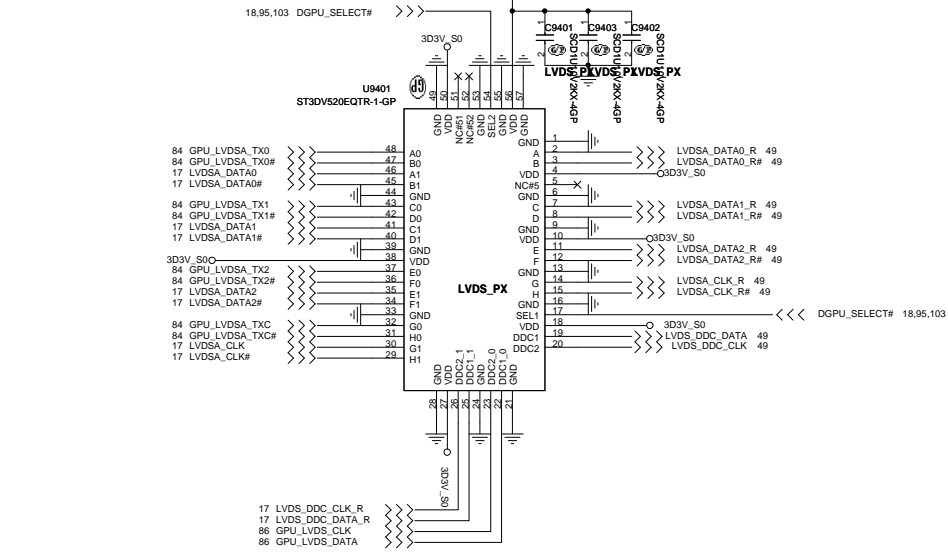


<Core Design>

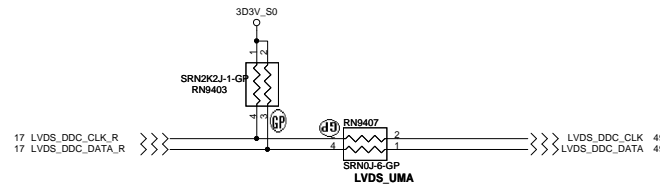
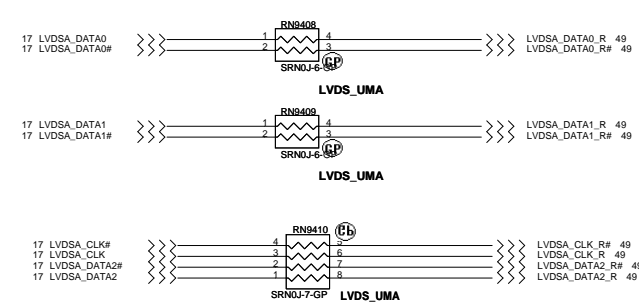
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DISCRETE VGA POWER			
Size Custom	Document Number		Rev
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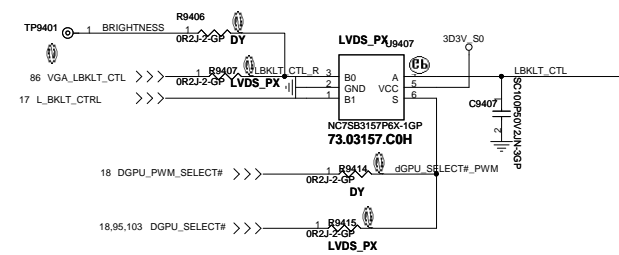
LVDS



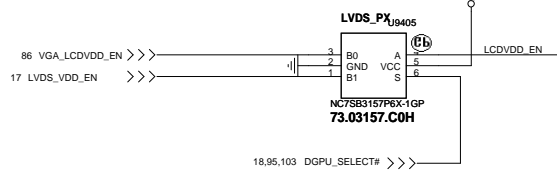
SEL->L(X=nX0),H(X=nX1)
SEL1 Control A~H
SEL2 Control DDC1,DDC2



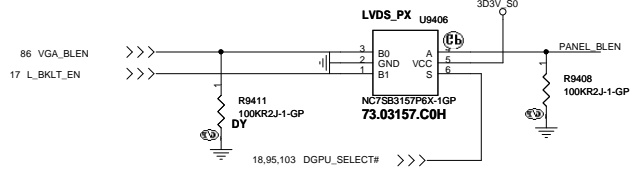
Panel BL brightness



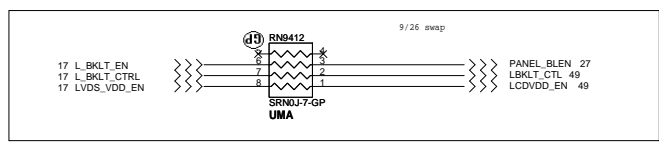
Power En



BL En



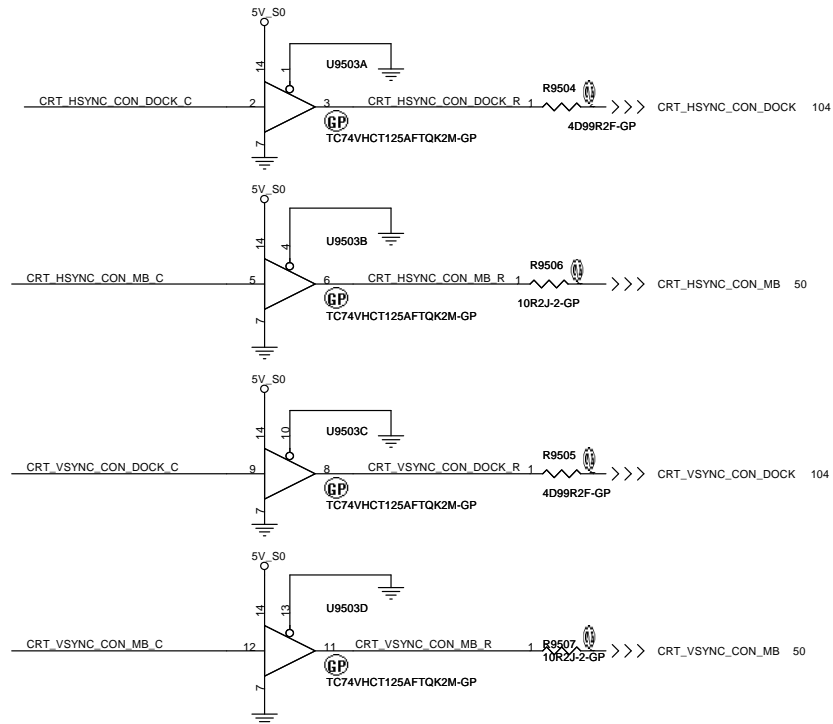
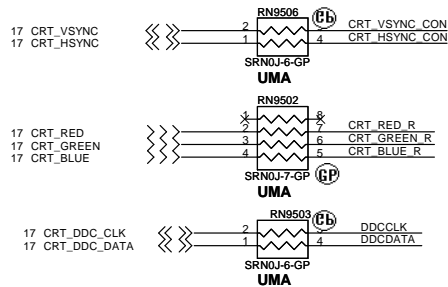
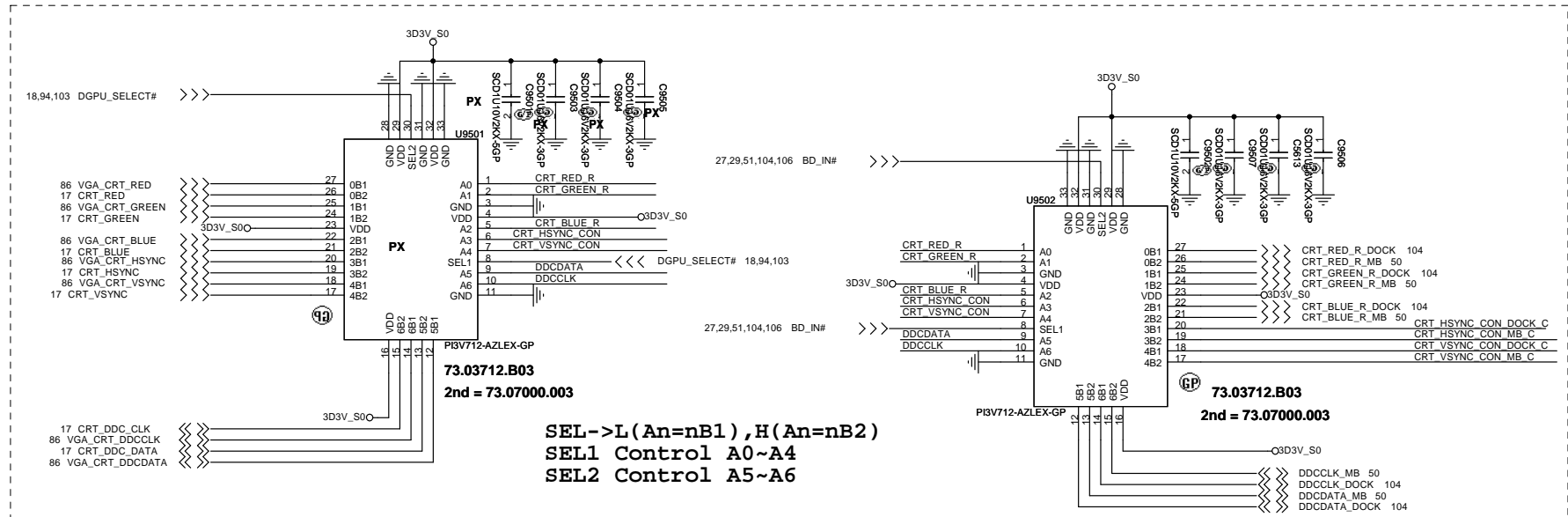
Panel BL brightness/Power En/BL En



CRT DDCDATA & DDCCLK

VDD :

Recommend to use 6 caps ($0.1\mu + 5 \times 10nF$) close to our chips



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Description	Date	Time	Location	Status
1	Title	Date	Time	Location	Status
2	Title	Date	Time	Location	Status
3	Title	Date	Time	Location	Status
4	Title	Date	Time	Location	Status
5	Title	Date	Time	Location	Status
6	Title	Date	Time	Location	Status
7	Title	Date	Time	Location	Status
8	Title	Date	Time	Location	Status
9	Title	Date	Time	Location	Status
10	Title	Date	Time	Location	Status
11	Title	Date	Time	Location	Status
12	Title	Date	Time	Location	Status
13	Title	Date	Time	Location	Status
14	Title	Date	Time	Location	Status
15	Title	Date	Time	Location	Status
16	Title	Date	Time	Location	Status
17	Title	Date	Time	Location	Status
18	Title	Date	Time	Location	Status
19	Title	Date	Time	Location	Status
20	Title	Date	Time	Location	Status
21	Title	Date	Time	Location	Status
22	Title	Date	Time	Location	Status
23	Title	Date	Time	Location	Status
24	Title	Date	Time	Location	

CRT Switch

Size

Document Number

BAD50-HC

Date: Saturday, March 03, 2012

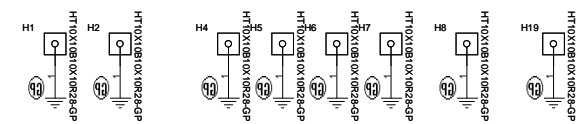
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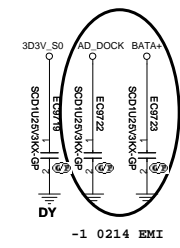
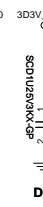
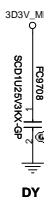
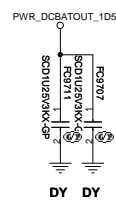
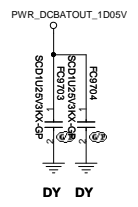
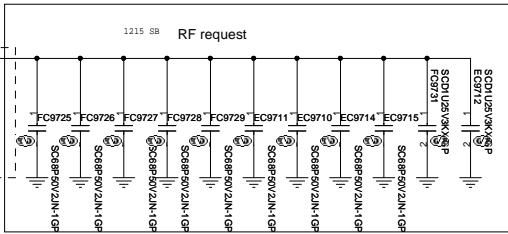
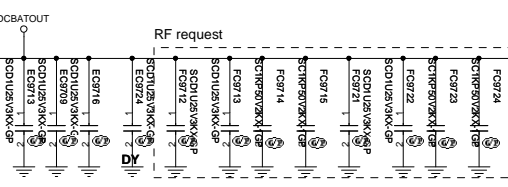
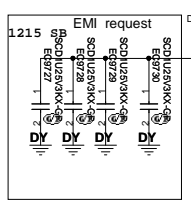
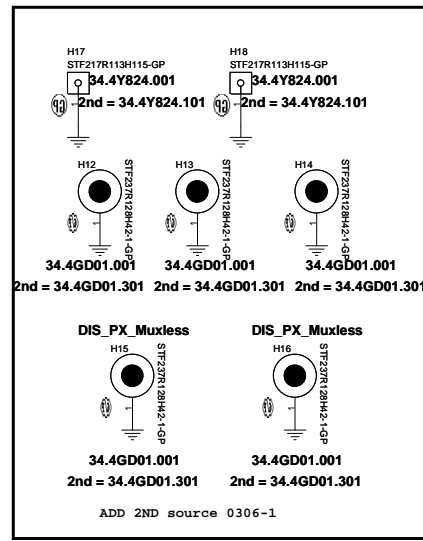
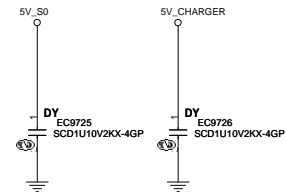
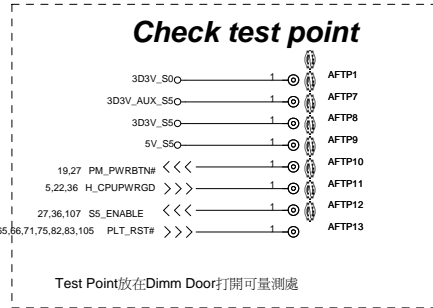
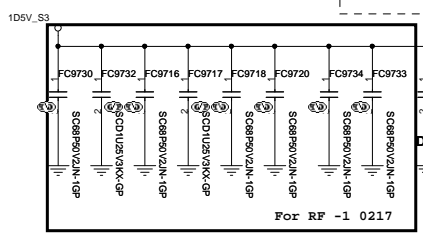
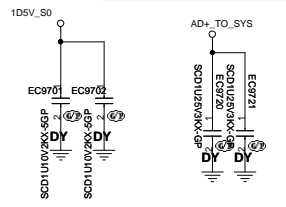
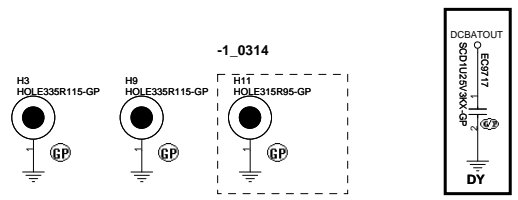
SSID = SDIO

<Core Design>

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		21F, 88, Sec.1, Hsin 1st Wu Rd., Hsinchu, Taipei Hsein 305, Taiwan, R.O.C.	
Title			
TOUCH PANEL			
Size A2	Document Number		Rev
	BAD50-HC		-1
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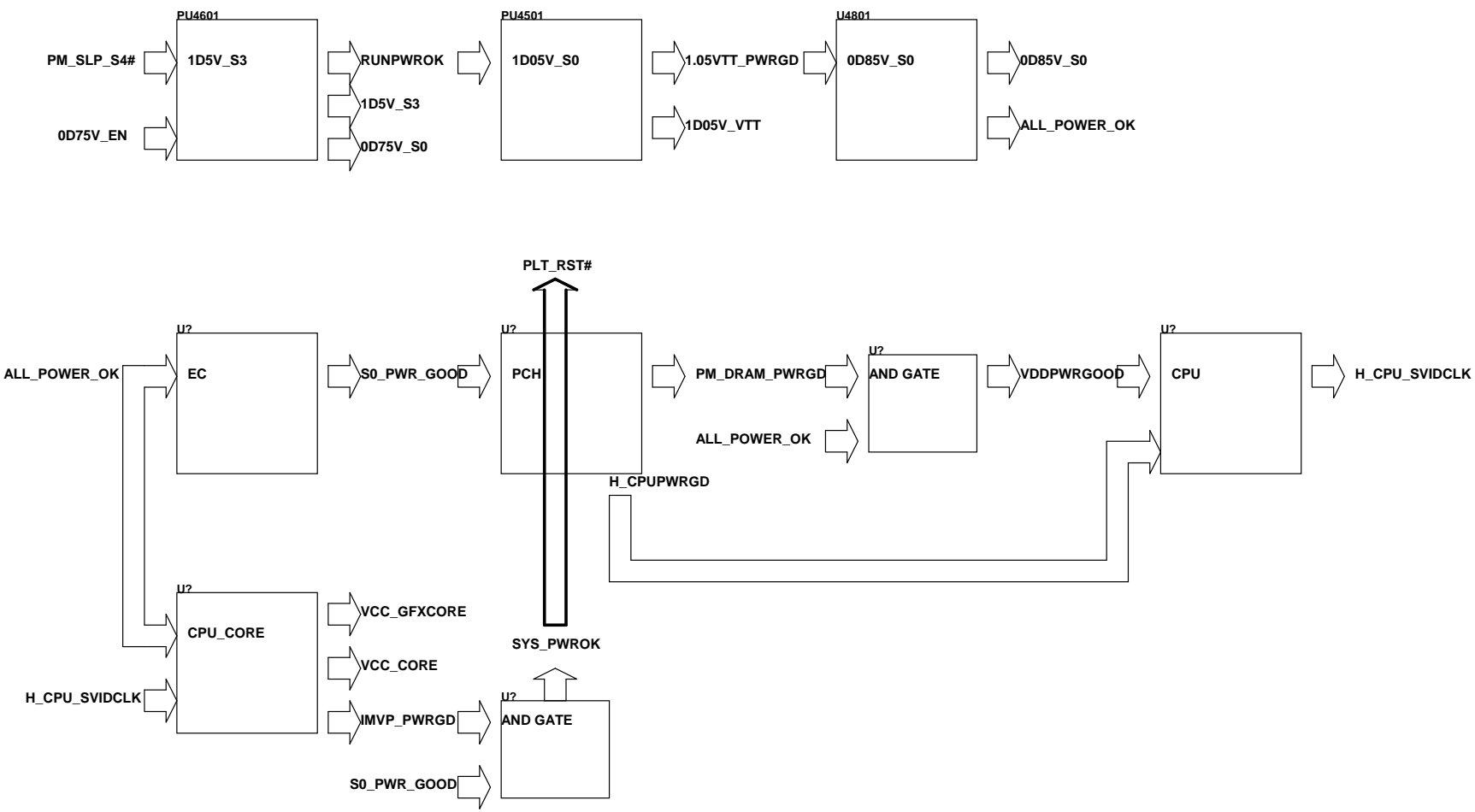


DEL Spring -1 0213



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Power Sequence

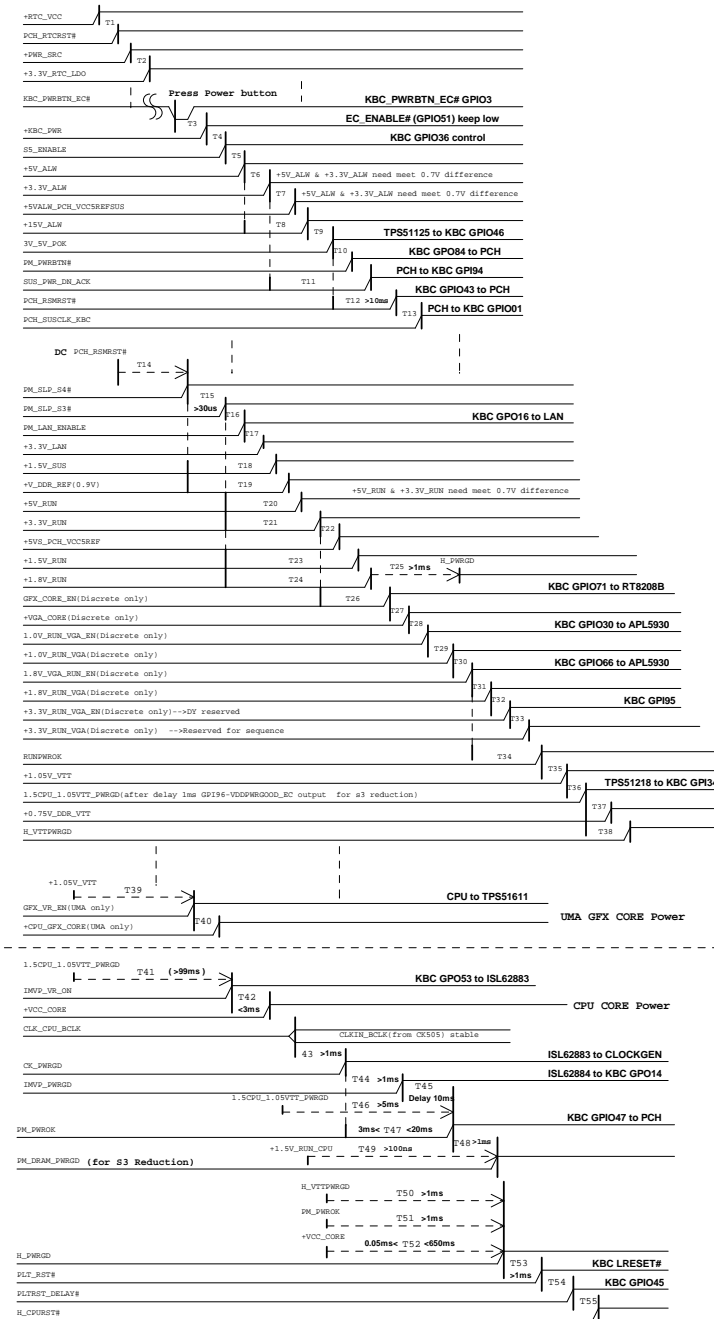


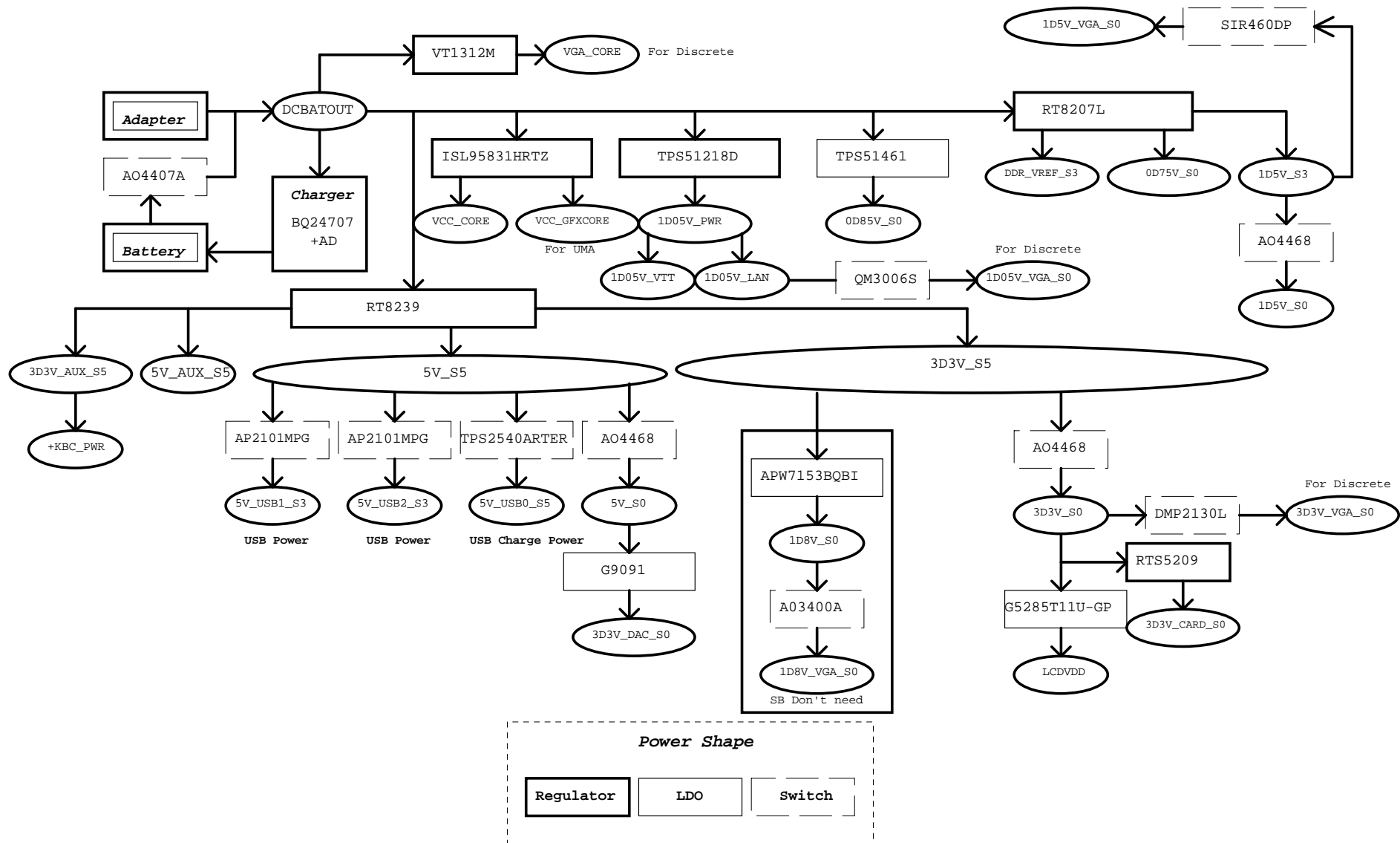
(AC mode)

The diagram illustrates the timing relationships between various signals during power-up and power-down sequences. Key signals and their timing constraints include:

- Power-Up Sequence:**
 - AC_PRESENT_BC** (T1) to **AC_PWRBTN_EC#** (T2): Delay $T1 - T2 > 10ms$.
 - AC_PWRBTN_EC#** (T2) to **AC_PWRBTN_EC#** (T3): Delay $T2 - T3 < 200ms$.
 - AC_PWRBTN_EC#** (T3) to **AC_PWRBTN_EC#** (T4): Delay $T3 - T4 > 30ms$.
 - AC_PWRBTN_EC#** (T4) to **AC_PWRBTN_EC#** (T5): Delay $T4 - T5 > 30ms$.
 - AC_PWRBTN_EC#** (T5) to **AC_PWRBTN_EC#** (T6): Delay $T5 - T6 > 30ms$.
 - AC_PWRBTN_EC#** (T6) to **AC_PWRBTN_EC#** (T7): Delay $T6 - T7 > 30ms$.
 - AC_PWRBTN_EC#** (T7) to **AC_PWRBTN_EC#** (T8): Delay $T7 - T8 > 30ms$.
 - AC_PWRBTN_EC#** (T8) to **AC_PWRBTN_EC#** (T9): Delay $T8 - T9 > 30ms$.
 - AC_PWRBTN_EC#** (T9) to **AC_PWRBTN_EC#** (T10): Delay $T9 - T10 > 30ms$.
 - AC_PWRBTN_EC#** (T10) to **AC_PWRBTN_EC#** (T11): Delay $T10 - T11 > 30ms$.
 - AC_PWRBTN_EC#** (T11) to **AC_PWRBTN_EC#** (T12): Delay $T11 - T12 > 30ms$.
 - AC_PWRBTN_EC#** (T12) to **AC_PWRBTN_EC#** (T13): Delay $T12 - T13 > 30ms$.
 - AC_PWRBTN_EC#** (T13) to **AC_PWRBTN_EC#** (T14): Delay $T13 - T14 > 30ms$.
 - AC_PWRBTN_EC#** (T14) to **AC_PWRBTN_EC#** (T15): Delay $T14 - T15 > 30ms$.
 - AC_PWRBTN_EC#** (T15) to **AC_PWRBTN_EC#** (T16): Delay $T15 - T16 > 30ms$.
 - AC_PWRBTN_EC#** (T16) to **AC_PWRBTN_EC#** (T17): Delay $T16 - T17 > 30ms$.
 - AC_PWRBTN_EC#** (T17) to **AC_PWRBTN_EC#** (T18): Delay $T17 - T18 > 30ms$.
 - AC_PWRBTN_EC#** (T18) to **AC_PWRBTN_EC#** (T19): Delay $T18 - T19 > 30ms$.
 - AC_PWRBTN_EC#** (T19) to **AC_PWRBTN_EC#** (T20): Delay $T19 - T20 > 30ms$.
 - AC_PWRBTN_EC#** (T20) to **AC_PWRBTN_EC#** (T21): Delay $T20 - T21 > 30ms$.
 - AC_PWRBTN_EC#** (T21) to **AC_PWRBTN_EC#** (T22): Delay $T21 - T22 > 30ms$.
 - AC_PWRBTN_EC#** (T22) to **AC_PWRBTN_EC#** (T23): Delay $T22 - T23 > 30ms$.
 - AC_PWRBTN_EC#** (T23) to **AC_PWRBTN_EC#** (T24): Delay $T23 - T24 > 30ms$.
 - AC_PWRBTN_EC#** (T24) to **AC_PWRBTN_EC#** (T25): Delay $T24 - T25 > 30ms$.
 - AC_PWRBTN_EC#** (T25) to **AC_PWRBTN_EC#** (T26): Delay $T25 - T26 > 30ms$.
 - AC_PWRBTN_EC#** (T26) to **AC_PWRBTN_EC#** (T27): Delay $T26 - T27 > 30ms$.
 - AC_PWRBTN_EC#** (T27) to **AC_PWRBTN_EC#** (T28): Delay $T27 - T28 > 30ms$.
 - AC_PWRBTN_EC#** (T28) to **AC_PWRBTN_EC#** (T29): Delay $T28 - T29 > 30ms$.
 - AC_PWRBTN_EC#** (T29) to **AC_PWRBTN_EC#** (T30): Delay $T29 - T30 > 30ms$.
 - AC_PWRBTN_EC#** (T30) to **AC_PWRBTN_EC#** (T31): Delay $T30 - T31 > 30ms$.
 - AC_PWRBTN_EC#** (T31) to **AC_PWRBTN_EC#** (T32): Delay $T31 - T32 > 30ms$.
 - AC_PWRBTN_EC#** (T32) to **AC_PWRBTN_EC#** (T33): Delay $T32 - T33 > 30ms$.
 - AC_PWRBTN_EC#** (T33) to **AC_PWRBTN_EC#** (T34): Delay $T33 - T34 > 30ms$.
 - AC_PWRBTN_EC#** (T34) to **AC_PWRBTN_EC#** (T35): Delay $T34 - T35 > 30ms$.
 - AC_PWRBTN_EC#** (T35) to **AC_PWRBTN_EC#** (T36): Delay $T35 - T36 > 30ms$.
 - AC_PWRBTN_EC#** (T36) to **AC_PWRBTN_EC#** (T37): Delay $T36 - T37 > 30ms$.
 - AC_PWRBTN_EC#** (T37) to **AC_PWRBTN_EC#** (T38): Delay $T37 - T38 > 30ms$.
 - AC_PWRBTN_EC#** (T38) to **AC_PWRBTN_EC#** (T39): Delay $T38 - T39 > 30ms$.
 - AC_PWRBTN_EC#** (T39) to **AC_PWRBTN_EC#** (T40): Delay $T39 - T40 > 30ms$.
 - AC_PWRBTN_EC#** (T40) to **AC_PWRBTN_EC#** (T41): Delay $T40 - T41 > 30ms$.
 - AC_PWRBTN_EC#** (T41) to **AC_PWRBTN_EC#** (T42): Delay $T41 - T42 > 30ms$.
 - AC_PWRBTN_EC#** (T42) to **AC_PWRBTN_EC#** (T43): Delay $T42 - T43 > 30ms$.
 - AC_PWRBTN_EC#** (T43) to **AC_PWRBTN_EC#** (T44): Delay $T43 - T44 > 30ms$.
 - AC_PWRBTN_EC#** (T44) to **AC_PWRBTN_EC#** (T45): Delay $T44 - T45 > 30ms$.
 - AC_PWRBTN_EC#** (T45) to **AC_PWRBTN_EC#** (T46): Delay $T45 - T46 > 30ms$.
 - AC_PWRBTN_EC#** (T46) to **AC_PWRBTN_EC#** (T47): Delay $T46 - T47 > 30ms$.
 - AC_PWRBTN_EC#** (T47) to **AC_PWRBTN_EC#** (T48): Delay $T47 - T48 > 30ms$.
 - AC_PWRBTN_EC#** (T48) to **AC_PWRBTN_EC#** (T49): Delay $T48 - T49 > 30ms$.
 - AC_PWRBTN_EC#** (T49) to **AC_PWRBTN_EC#** (T50): Delay $T49 - T50 > 30ms$.
 - AC_PWRBTN_EC#** (T50) to **AC_PWRBTN_EC#** (T51): Delay $T50 - T51 > 30ms$.
 - AC_PWRBTN_EC#** (T51) to **AC_PWRBTN_EC#** (T52): Delay $T51 - T52 > 30ms$.
 - AC_PWRBTN_EC#** (T52) to **AC_PWRBTN_EC#** (T53): Delay $T52 - T53 > 30ms$.
 - AC_PWRBTN_EC#** (T53) to **AC_PWRBTN_EC#** (T54): Delay $T53 - T54 > 30ms$.
 - AC_PWRBTN_EC#** (T54) to **AC_PWRBTN_EC#** (T55): Delay $T54 - T55 > 30ms$.
- Power-Down Sequence:**
 - AC_PWRBTN_EC#** (T1) to **AC_PWRBTN_EC#** (T2): Delay $T1 - T2 > 10ms$.
 - AC_PWRBTN_EC#** (T2) to **AC_PWRBTN_EC#** (T3): Delay $T2 - T3 < 200ms$.
 - AC_PWRBTN_EC#** (T3) to **AC_PWRBTN_EC#** (T4): Delay $T3 - T4 > 30ms$.
 - AC_PWRBTN_EC#** (T4) to **AC_PWRBTN_EC#** (T5): Delay $T4 - T5 > 30ms$.
 - AC_PWRBTN_EC#** (T5) to **AC_PWRBTN_EC#** (T6): Delay $T5 - T6 > 30ms$.
 - AC_PWRBTN_EC#** (T6) to **AC_PWRBTN_EC#** (T7): Delay $T6 - T7 > 30ms$.
 - AC_PWRBTN_EC#** (T7) to **AC_PWRBTN_EC#** (T8): Delay $T7 - T8 > 30ms$.
 - AC_PWRBTN_EC#** (T8) to **AC_PWRBTN_EC#** (T9): Delay $T8 - T9 > 30ms$.
 - AC_PWRBTN_EC#** (T9) to **AC_PWRBTN_EC#** (T10): Delay $T9 - T10 > 30ms$.
 - AC_PWRBTN_EC#** (T10) to **AC_PWRBTN_EC#** (T11): Delay $T10 - T11 > 30ms$.
 - AC_PWRBTN_EC#** (T11) to **AC_PWRBTN_EC#** (T12): Delay $T11 - T12 > 30ms$.
 - AC_PWRBTN_EC#** (T12) to **AC_PWRBTN_EC#** (T13): Delay $T12 - T13 > 30ms$.
 - AC_PWRBTN_EC#** (T13) to **AC_PWRBTN_EC#** (T14): Delay $T13 - T14 > 30ms$.
 - AC_PWRBTN_EC#** (T14) to **AC_PWRBTN_EC#** (T15): Delay $T14 - T15 > 30ms$.
 - AC_PWRBTN_EC#** (T15) to **AC_PWRBTN_EC#** (T16): Delay $T15 - T16 > 30ms$.
 - <

red word: KBC GPIO

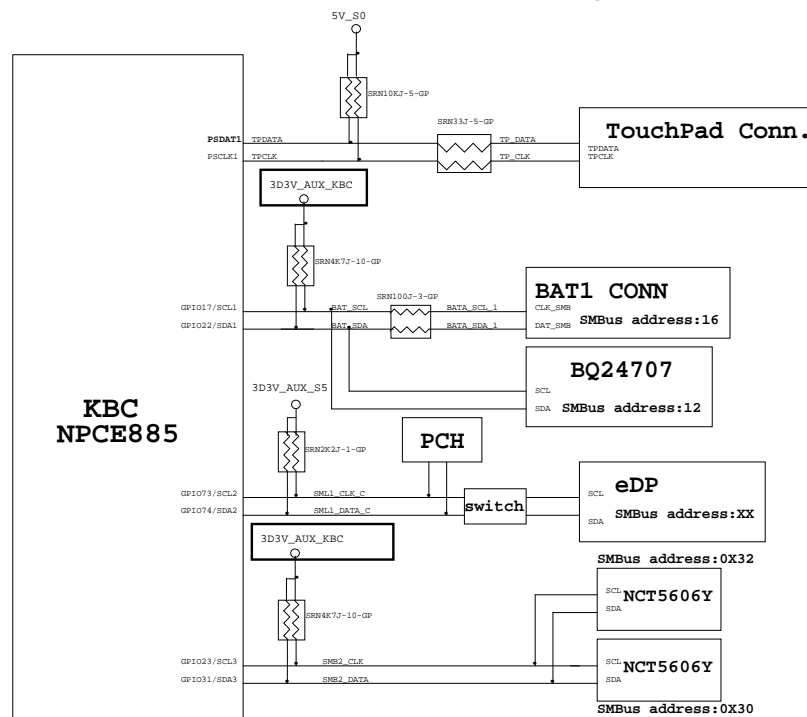




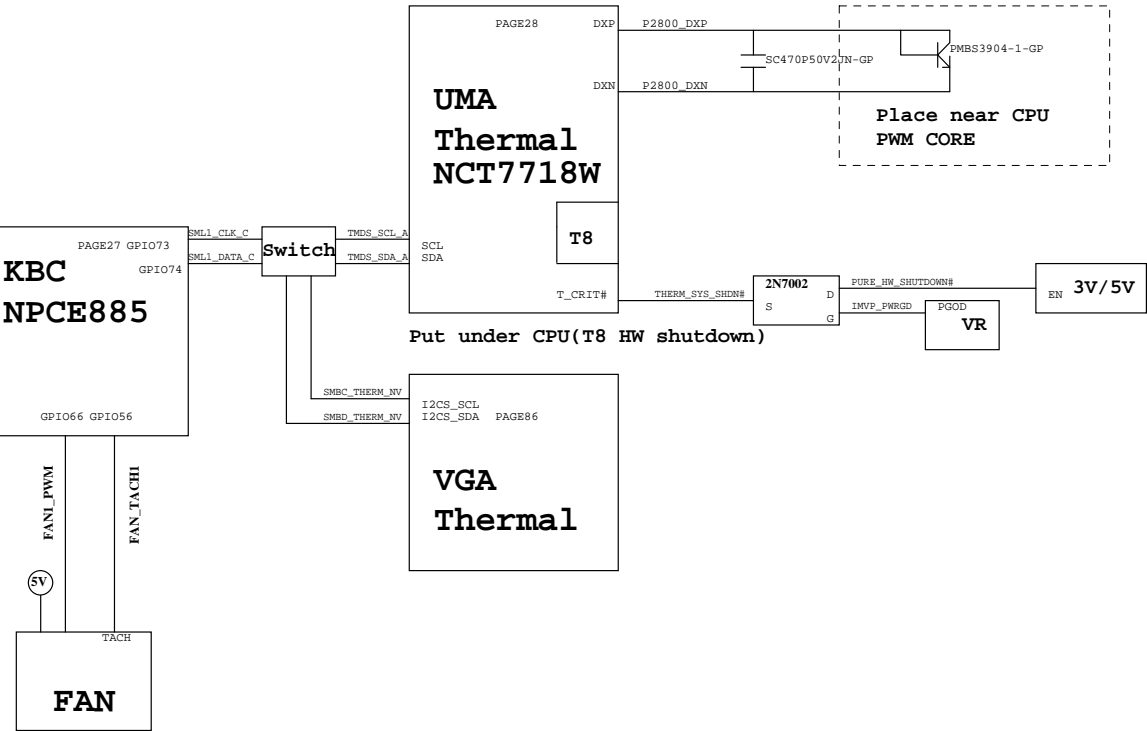
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power Block Diagram	
Size A3	Document Number BAD50-HC
Date: Saturday, March 03, 2012	Rev -1
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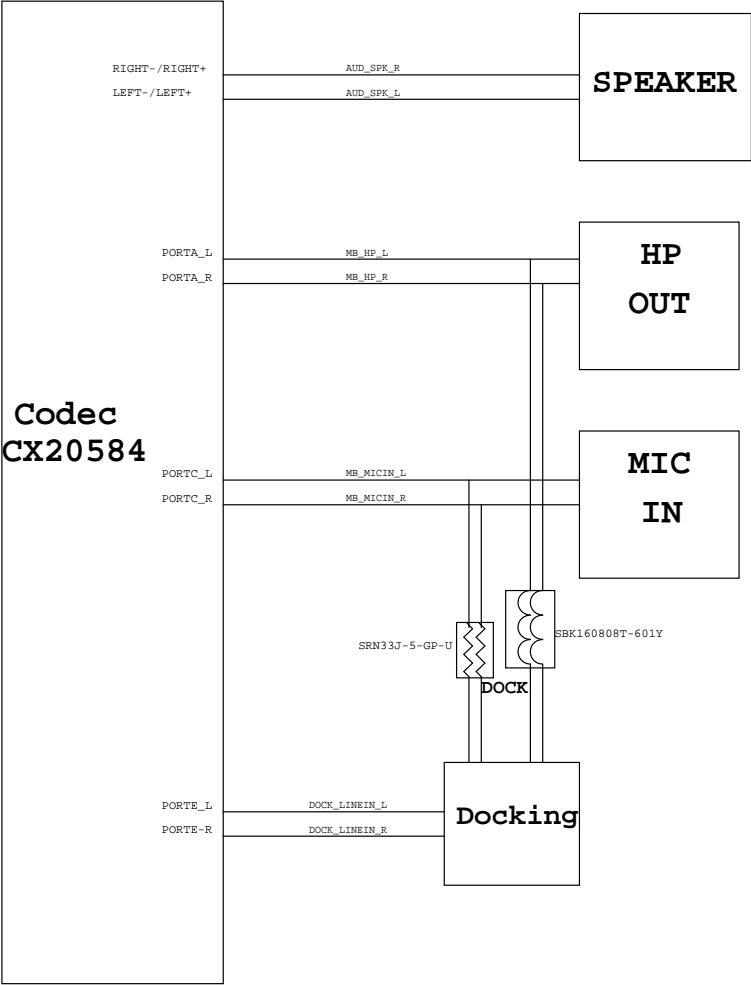
KBC SMBus Block Diagram

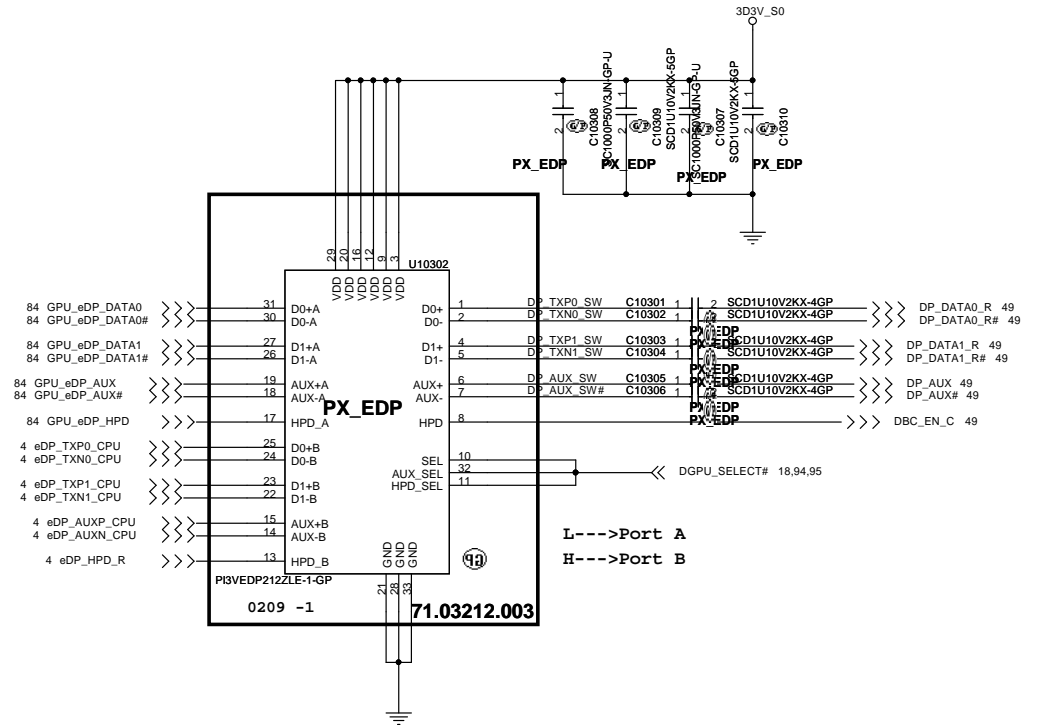
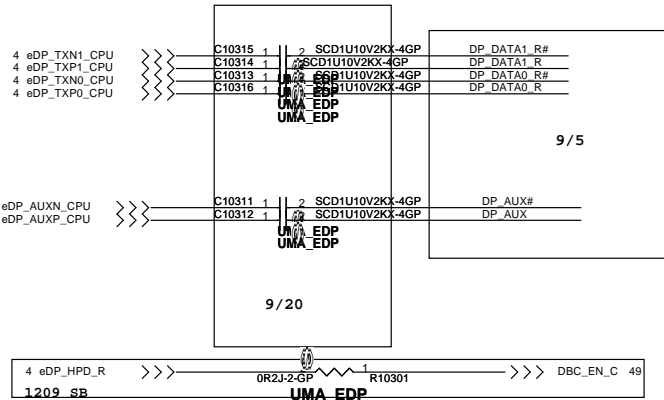


Thermal Block Diagram

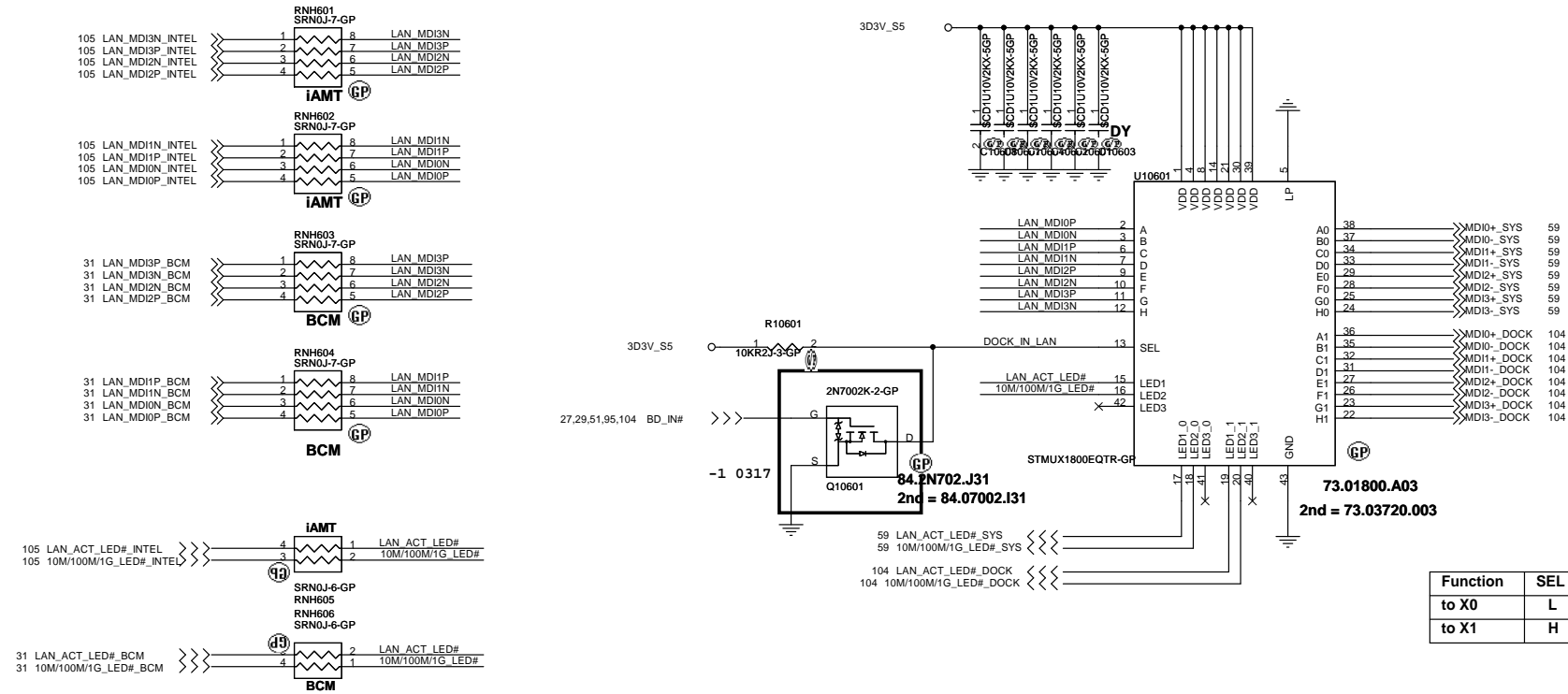


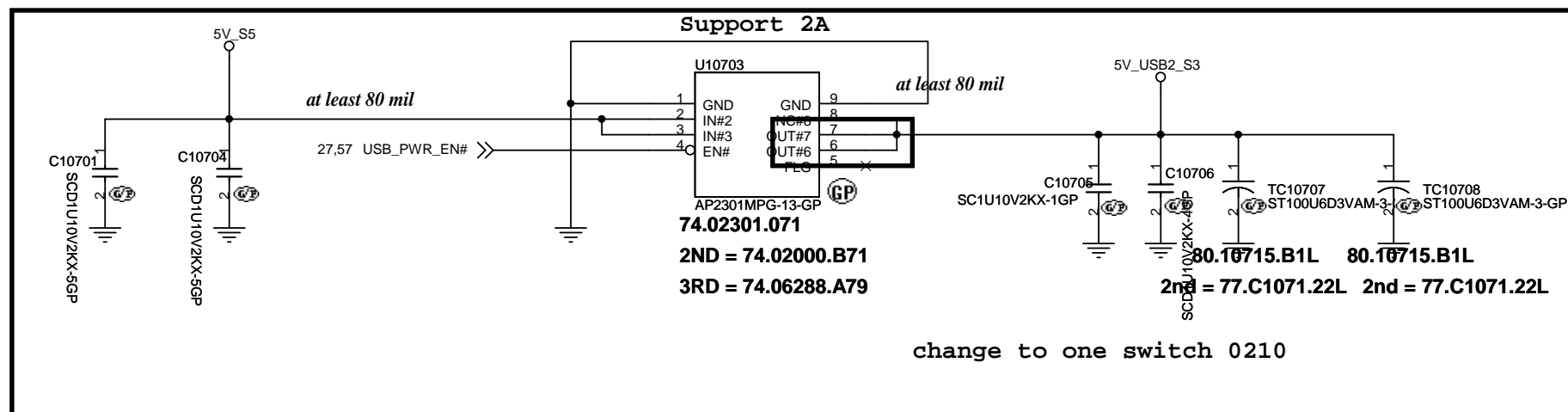
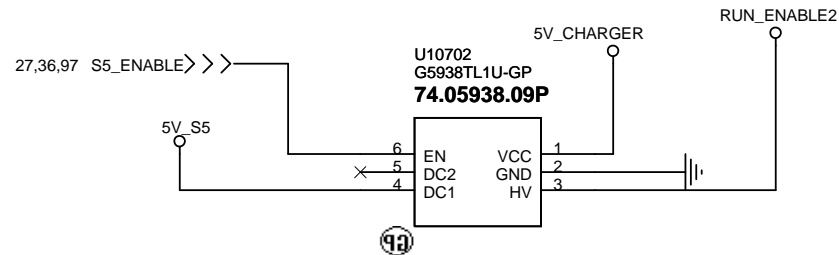
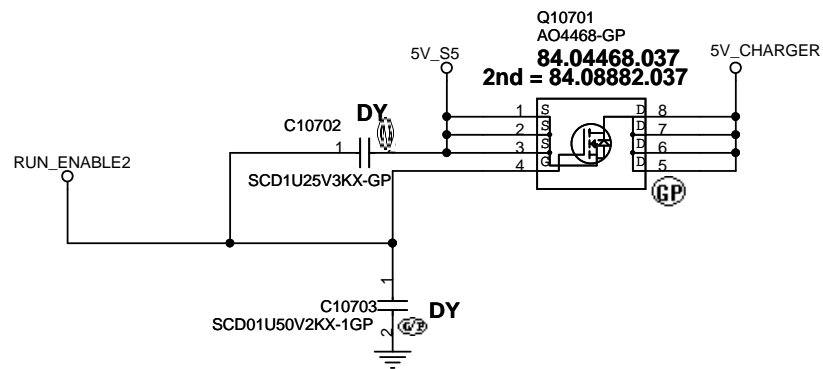
Audio Block Diagram





LAN switch





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USB charger			
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I2C mode
To USB BD

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Title			
USB30 re-driver			
Size	Document Number		Rev
B	BAD50-HC		-1
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